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Low-Cost Driver for SEMITOP® Inverter

Introduction

An increasing number of manufacturers of motor control and UPS systems are replacing their discrete power devices (in TO packaging) with integrated power modules to improve the performance and reliability of their systems. SEMITOP is a versatile "baseplateless" power module that boasts high-level integration capability and is suitable for both consumer and industrial applications. Single-screw mounting and through-hole soldering PINs make this device the best solution for motion control (fan, pump and motor drives) and UPS systems where system integration and increased performance are called for. SEMITOP® is often selected by design engineers as an alternative solution to IPMs. This Application Note is a technical reference to assist designers in developing systems with an integrated SEMITOP® six-pack power module that boast greater flexibility than IPMs. A general-purpose low-cost motor drive solution using the bootstrap principle has been chosen for this purpose.

1. Product description

SEMIKRON has developed a low-cost PCB demo board based on the bootstrap principle. In order to keep costs low and the design relatively simple, all of the devices chosen for this demo board are standard components. The application-specific HVIC used for this design, the core of the board, is the L6386 from STMicroelectronics, which has sufficient output peak current capability to drive the latest-generation NPT-IGBT used in SEMITOP® modules.

The main features of the driver are:

- High-voltage high-speed level shifting
- Control circuit under-voltage (UV) protection
- Short circuit protection (SC)
- Fault signals (SC fault or UV fault)
- Fault signal timing adjustment
- CMOS/TTL input logic level compatibility
- NTC temperature monitoring
- Over-temperature (OT) protection

The power module used in this demo board is the new three-phase IGBT inverter SK35GD065ET in SEMITOP® 3 housing. The internal circuit topology (shown in Fig.1) features bottom IGBTs with open emitters. The driver can easily be used in for both control technique in AC induction motors: Vector control (three separate current shunts) and V per Hz control (with only one current shunt). Moreover, it can easily be used for both types of AC motor (induction motors and synchronous motors), as well as BLDC motors. This driver is also suitable, however, for UPS systems. In particular, the topology described here features one sense resistor only. This can, however, easily be extended to three current sensors, if desired.

Fig. 2 and Table 1 show the complete schematic of the driver and the related parts list.

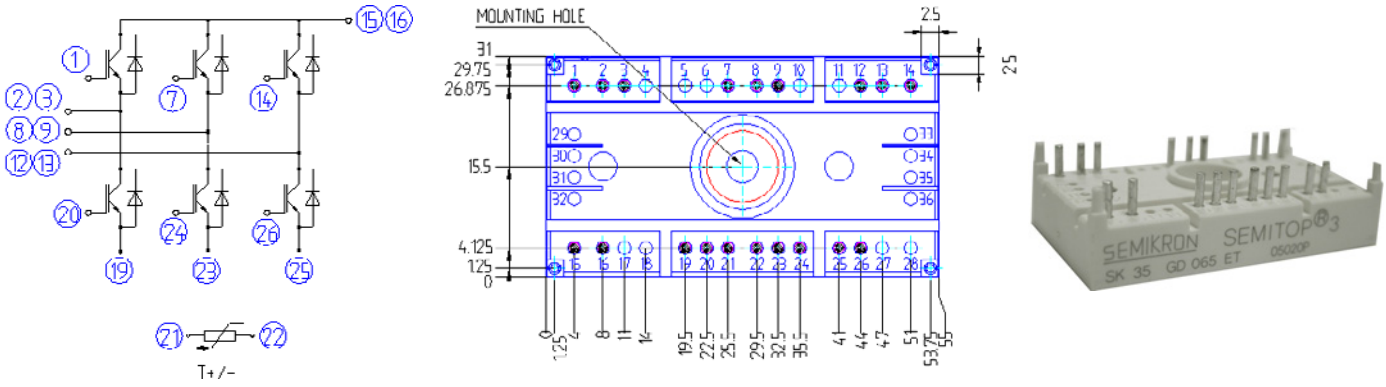


Figure 1: Electrical circuit, outline dimensions and housing of SK 35 GD 065ET

As mentioned above, the driver technique is based on level shift technology in order to achieve a balance between cost and performance. In fact, driving the latest-generation NPT IGBT with gate-emitter voltages ($\mathbf{V_{GE}}$) between 0 and 15V instead of the typical –8V/+15V means an increase in switching losses of between 5 and 10 %. The benefits, however, and, in particular, the cost savings achievable with the use of only one ground referenced voltage source rather than a minimum of four complicated insulated independent DC/DC power supplies are immense. A number of devices can be removed, saving room in the PCB and simplifying the design. This is mainly due to the input logic, drivers and power stage, which have the same ground reference. In fact, the demo board is assembled on a small PCB, which allows for a considerable space and hence cost reduction.

2. System features

2.1 Inverse polarity protection

In order to prevent damage in the event of incorrect power supply connection/operation (see Fig. 2, PIN V_{CC} and PIN ground, i.e. PIN PC), the driver is protected against inverse polarity. The absolute maximum permissible reverse input voltage between V_{CC} and ground is 30V. The maximum reverse current in such conditions is 10µA.

2.2 Input signals

Thanks to the input interfaces, the driver can accept six PWM signals in TTL and CMOS logic level. That means the input logic level accepted lies between 3V and 15V. Six PWM input signals in phase with the output stage can drive each IGBT inside the SEMITOP® module independently. Owing to this approach, the driver is suitable for several motor loads (AC IM, BLDCM, IPM, SPM…). This also means that the customer can easily connect his control unit (CPU or application-specific IC based control unit) to the driver without any isolation interface (using opto-couplers or transformers).

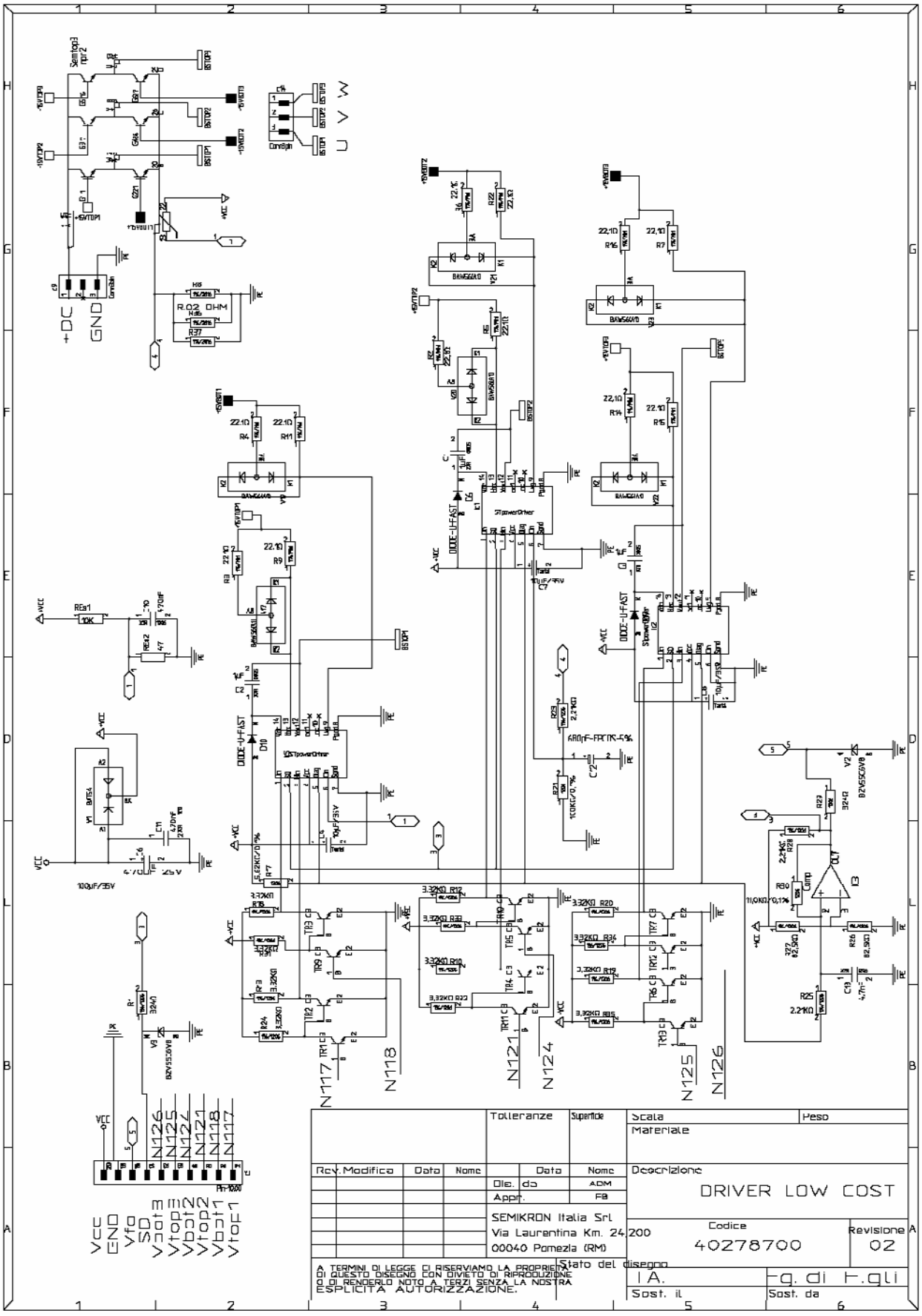


Figure 2: Driver Schematic

	Bill of materials 40278700-02		
C1 805 ceramic	1µF/25V /10%	R27-1206-0.25W	82.5K 1%
C2 805 ceramic	1µF/25V /10%	R28-1206-0.25W	2.2 K 1%
C3 805 ceramic	1µF/25V /10%	R29-1206 0.25W	330ohm 2%
C4-Tantalum Electr\CASE D	10µF/35V /10%	R30-1206	11.0K not to mount
C6- 2,5/6,3/11,2 Elect	100µF/35V /20%	R31-1206 0.25W	3.32K 2%
C7-Tantalum Electr\CASE D	10µF/35V /10%	R32-1206 0.25W	3.32K 2%
C8-Tantalum Electr\CASE D	10µF/35V /10%	R33-1206 0.25w	3.32K 2%
C10-1206 Ceramic	470nF/25V /10%	R34-1206 0.25W	3.32K 2%
C11-1210 Tantalum	470nF/35V /10%	R35-1206 0.25w	3.32K 2%
C12-1206 Ceramic	680pF/50V /10%	R36-Isabellenhuette 3W	SMT R100-1 1%
C13-1206 Ceramic	4.7nF/50V /10%	R37-Isabellenhuette 3W	SMT R100-1 1%
D6-DO214AC(SMA)	ES1D Diode ultra fast	REs1-1206	3.3K 1%
D7 DO214AC(SMA)	ES1D Diode ultra fast	REs2-1206	22 ohm 1%
D10 DO214AC(SMA)	ES1D Diode ultra fast	TR1NPN A8F npn sot23	MMUN2216LT1
IC3-SO8	LM311	TR2NPN A8F npn sot23	MMUN2216LT1
R1 - 1206-0.25W	330ohm 1%	TR3NPN A8F npn sot23	MMUN2216LT1
R2 - 1206-0.25W	22 ohm 1%	TR4NPN A8F npn sot23	MMUN2216LT1
R3 - 1206-0.25W	22 ohm 1%	TR5NPN A8F npn sot23	MMUN2216LT1
R4 - 1206-0.25W	22 ohm 1%	TR6NPN A8F npn sot23	MMUN2216LT1
R5 - 1206-0.25W	22 ohm 1%	TR7NPN A8F npn sot23	MMUN2216LT1
R6 - 1206-0.25W	22 ohm 1%	TR9NPN A8F npn sot23	MMUN2216LT1
R7 -1206-0.25W	22 ohm 1%	TR10NPN A8F npn sot23	MMUN2216LT1
R8 -Isabellenhuette 3W	SMT R100-1 1%	TR11NPN A8F npn sot23	MMUN2216LT1
R9 -1206-0.25W	22 ohm 1%	TR12NPN A8F npn sot23	MMUN2216LT1
R10 -1206-0.25W	3.3K 2%	TR13NPN A8F npn sot23	MMUN2216LT1
R11 -1206-0.25W	22 ohm 1%	V1	BAT54C
R12 -1206-0.25W	3.32K 2%	V2 Zener	BZV55C5V6
R13 -1206-0.25W	3.32K 2%	V3 Zener	BZV55C5V6
R14-1206-0.25W	22 ohm 1%	V17	BAW56(A1)
R15 -1206-0.25W	22 ohm 1%	V19	BAW56(A1)
R16 -1206-0.25W	22.1ohm 1%	V20	BAW56(A1)
R17 -1206-0.25W	5.1K 2%	V21	BAW56(A1)
R18-1206-0.25W	3.32K 2%	V22	BAW56(A1)
R19-1206-0.25W	3.32K 2%	V23	BAW56(A1)
R20 1206-0.25W	3.32K 2%	ic1	ic1 L6386:SO14
R21 -1206-0.25W	100K 5%	ic2	ic2 L6386:SO14
R22 -1206-0.25W	22 ohm 1%	ic5	ic5 L6386:SO14
R23 1206-0.25W	2.2K 1%	npn2(SEMITOP3)	SK35GD065ET
R24-1206-0.25W	3.3K 2%	c5 passo 2.54mm Fila sing.10poli	
R25-1206-0.25W	2.2K 1%	c9 Mors.passo 7.62 3poli	
R26-1206-0.25W	82.5K 1%	c14 Mors.passo 7.62 3 poli	

Table 1: Parts list for the low-cost driver

2.3. Over-current protection

Over-current protection is provided by a sense resistor connected between ground and power module (PINs 19, 23 and 25 connected together). The value of this resistor defines the over-current limit. As shown in Fig. 2, the fast over-current protection circuit is based on only one application, working on the voltage divider R_{23} and R_{21}. integrated comparator in the L6386 and a resistive divider. This is to prevent the current flow across the sense resistor from reaching dangerous values. The customer can easily choose the optimum value for his

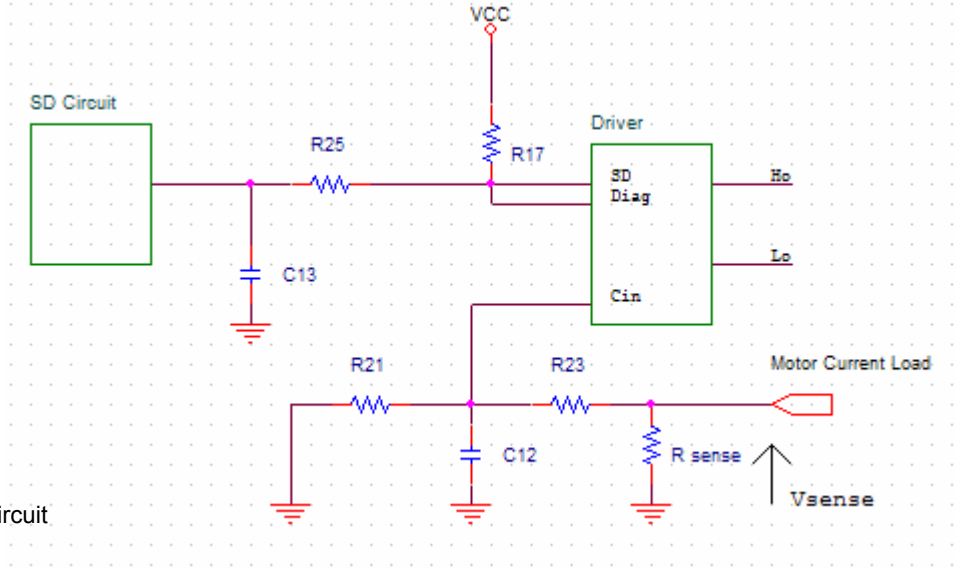


Figure 3: Over-current protection circuit

From the electrical circuit, the current limit threshold, I_{limit}, of the power module is defined as:

$$I_{limit} = 0.5 \cdot \frac{R_{23} + R_{21}}{R_{sense} \cdot R_{21}}$$

Varying the R_{sense} value will change I_{limit} only, since the internal threshold is 0.5, meaning that the current protection circuit will switch on when the voltage drop across R_{sense} is:

$$R_{sense} \cdot I_{limit} > 0.5 \cdot \frac{R_{23} + R_{21}}{R_{21}}$$

If the voltage drop $R_{sense} \cdot I_{limit}$ is higher than the set threshold level, the voltage across the ASIC L6386 diagnostic PIN (DIAG) as well as the shutdown PIN (SD) is switched at a low level. In this case the output will be switched off. The output will be kept switched off until the SD PIN level is high. The delay time between the fault condition and reset depends on the timing capacitor C_{13}. The reset time constant τ_{reset} can be set by varying the timing capacitor C_{13} and the resistance net R_{17} and R_{25}, while the active shutdown time constant depends on C_{13} and R_{25}. As a result, changing C_{13} makes it possible to change the two time constants.

2.4. Over-temperature protection

With the integrated NTC temperature sensor (KG3B-35) inside the SEMITOP® (between PINs 21 and 22), it is possible to monitor the upper DBC temperature level. With the use of external circuitry, it is possible to provide accurate over-current protection.
Figure 4 shows the schematic drawing of the over-temperature protection circuit.

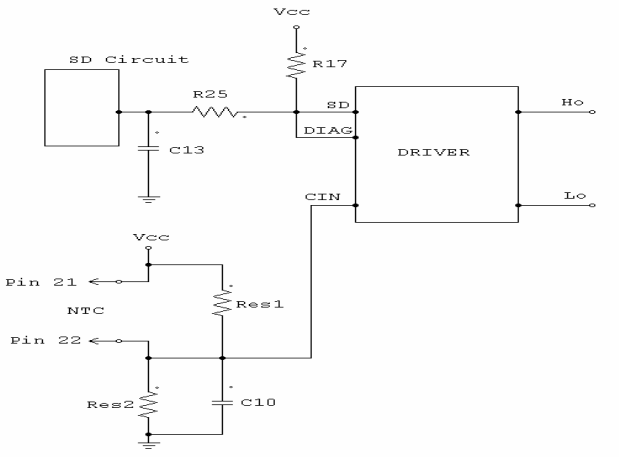


Figure 4: Over-temperature protection circuit

The NTC temperature sensor exhibits a non-linear R/T characteristic. To provide a correlation between the resistance value and the threshold limit of the over-temperature protection, a linear characteristic is needed. For this purpose, a resistance is used in parallel to the NTC. To understand how it is possible to change the NTC characteristic, the expression of the NTC resistance for different temperature values will be analysed. The NTC resistance can be expressed as:

$$R(T_2) = R_{T_1} \cdot e^{[B\cdot(\frac{1}{T_2}-\frac{1}{T_1})]}$$

Where R_{T1} is the NTC resistance measured for a temperature of T_1; R_{T2} is the NTC resistance value measured for a temperature of T_2; B is the typical NTC value (expressed in K).

The B value is not constant, but is directly dependent on the temperature. For a temperature range from 25°C to 85°C, B value can be considered constant, meaning that the R(T) value can be easily determined. If a resistance R_p is used in parallel with NTC, the total resistance obtained will be:

$$R_{total(T)} = \frac{R_{NTC}(T)\cdot R_p}{R_{NTC}(T)+R_p}$$

The best linearization is achieved by putting the turning point in the middle of the operating temperature range. It can be supposed that the operating temperature range is between 25°C and 80°C, meaning that the middle point would be 52.5°C. The NTC value for a temperature of 52.5°C is 1897Ω. The best R_p value can therefore be calculated as follows:

$$R_p = R_{NTC\_25}\cdot\frac{B-2\cdot T}{B+2\cdot T}$$

For a temperature of 25°C, the NTC resistance is 5kΩ and B is 3420K. Substituting the previous equation would result in:

$$R_p = 5\cdot 10^3 \cdot \frac{3420-(2\cdot(52.5+273.15))}{3420+(2\cdot(52.5+273.15))} \cong 3400\Omega$$

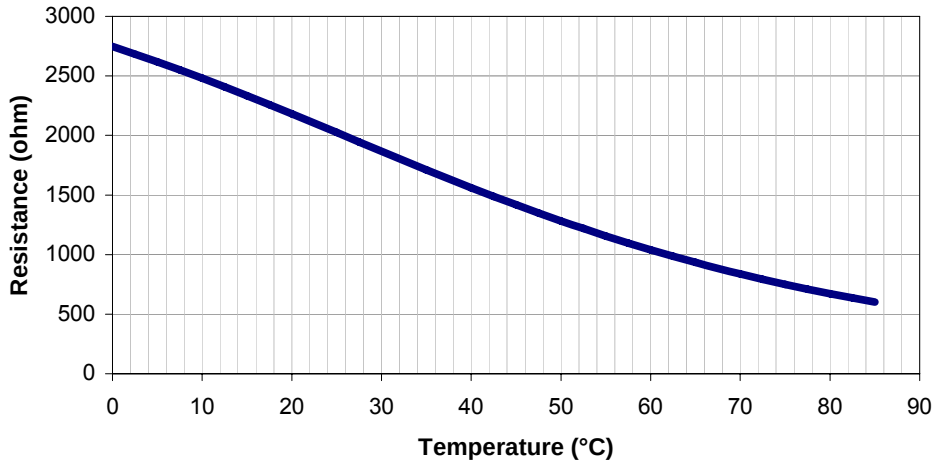


Figure 5: NTC resistance vs. temperature (modified)

The thermal protection shuts down the devices when the temperature reaches 82.5°C; this value corresponds to an R_{total} min of 636Ω. In this case, the voltage drop across R_{es2} reaches 0.5V, which is the threshold voltage level of the over-temperature protection. The behaviour is the same as described for the over-current protection, but the shutdown condition is different. In fact, the device will be kept in shutdown until the temperature is under the upper limit. The position of the NTC sensor inside the SEMITOP® module makes this type of protection very effective.

2.5. Over-voltage protection

Over-voltage protection is ensured by the intervention of the over-voltage limit of the ASIC L6386. The voltage window of UVLO intervention is between 10 and 12V. The UVLO will switch off the ASIC when the power supply is lower than 10V. The fault condition is not reset until the power supply is higher than 12V.

Bootstrap capacitor dimensioning

The correct dimensioning of the bootstrap capacitor is really important in the design of this low-cost driver, since this device is the heart of the bootstrap principle. The bootstrap capacitor is connected to the L6386 power supply by an external bootstrap diode. This diode is used to charge the capacitor every time the low-side driver is switched on (the L6386 has an integrated bootstrap diode, but its internal series resistance r_T=125Ω is too high to be used in SEMITOP® applications; for this reason it has been used an external diode with r_T=1Ω in the demo board).

When the low-side driver is off, the voltage between the cathode of the bootstrap diode and ground is higher than the anode, meaning the diode is off. The capacitor is not discharged until the high-side switch is turned on, and the charge is used to supply the input capacitance of the switch itself. Fig. 6 shows the electrical circuit of the bootstrap section when the low side is on.

A method of setting the right value for the bootstrap capacitor and matching it with different IGBT sizes is described below.

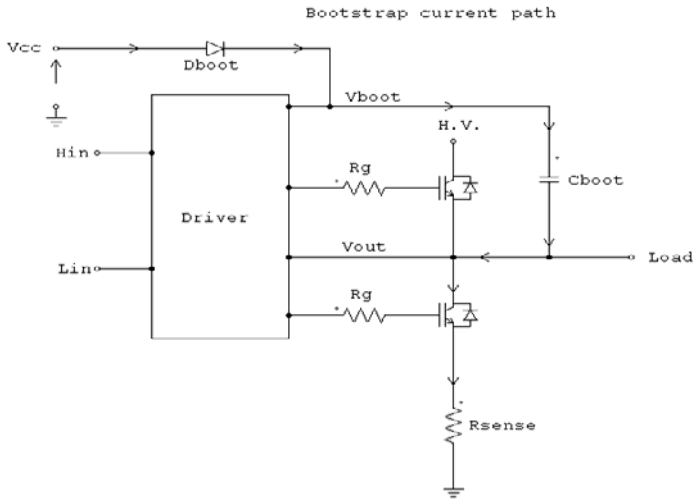


Figure 6: Bootstrap capacitor charging path

An important parameter to take into consideration is the voltage drop ΔV_{boot}, which has to be guaranteed when the high-side switch is turned on. As shown in Fig. 6, the voltage drop ΔV_{boot} depends on the IC power supply (V_{CC}), the forward voltage of the diode (V_F) and the minimum gate-to-emitter voltage (V_{ge_min}):

$$\Delta V_{boot} = V_{cc} - V_f - V_{ge\_min}$$

Hence, to obtain the capacitor size value, we can use the following equation:

$$C_{boot} = \frac{Q_{boot}}{\Delta V_{boot}}$$

where a duty cycle of 50% is assumed.

where Q_{boot} is the total charge that has to be supplied by the capacitor Q_{boot} and depends on several factors: high-side switch total gate Q_{gate}; high-side switch gate-to-source leakage current I_{gate_lkg} ; bootstrap capacitor leakage current I_{boot_lkg} ; bootstrap quiescent current of the ASIC I_{qs_ic}; bootstrap leakage current of the IC I_{lkg_ic} ; charge required for the level shifter of the IC Q_{lsf} ; high-side switch-on time t_{on} and diode leakage current I_{d_lkg}.

The total charge supplied from the bootstrap capacitor is:

$$Q_{boot} = Q_{gate} + (I_{gate\_lkg} + I_{boot\_lkg} + I_{qs\_ic} + I_{lkg\_ic} + I_{d\_lkg}) \cdot t_{on} + Q_{lsf}$$

For the SEMITOP® SK35GD065ET used in this demo board, the results are: Q_{gate}=130nC, I_{gate_lkg}=120nA, I_{qs_ic}=200µA, I_{lkg_ic}=10µA, Q_{lsf}=3nC, t_{on}=100µs, I_{d_lkg}=10nA. Assuming a maximum voltage drop of 0.15V (1% of the power supply), the size of the bootstrap capacitor will be:

$$C_{boot} = \frac{154nC}{0.15V} = 1\mu F$$

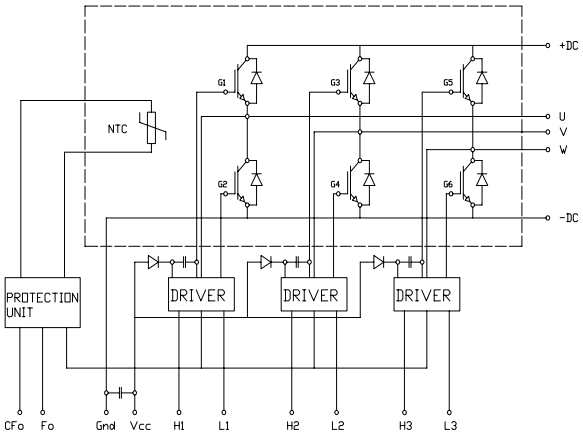


Figure 6: functional block diagram

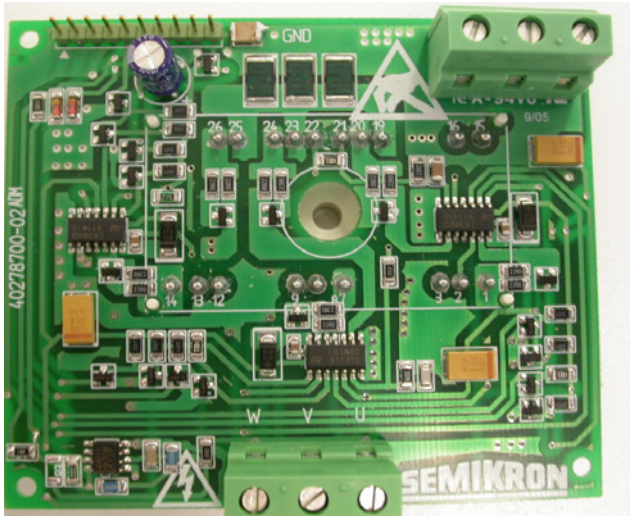


Figure 7: PCB demo board (top side)

4. Test results

Several tests have been carried out on the demo board to verify the functionality in actual application for different environments and load conditions.
***Test equipment**:* Single-phase input bridge rectifier, DC link capacitor bank (properly connected as close as possible to the demo board), three-phase induction motors with different power ratings from 0.2 up to 2.25kW as loads, DSP based 3-Ø AC IM control, DC Voltage supply.
***Monitoring equipment**:* LT374 LeCroy oscilloscope, CP150 LeCroy current probes, ADP300 LeCroy differential voltage probes, Tektronix oscilloscope, LEM current sensors, temperature sensors.

4.1. Test conditions

The DC voltage obtained in the tests (i.e. 330V) was obtained by rectifying the 1-Ø 50Hz 230V_{ac} and filtering it with a purpose designed filter capacitor bank (seven film capacitors 0.22µF/600V each in parallel with 8000µF/450V electrolytic capacitors and connected to the demo board by bus bar and placed as close as possible to the SEMITOP® DC PIN and GND PINs; i.e. SEMITOP® PIN 15 and demo board PIN GND). The power supply V_{CC} is 15V and the DSP switching frequency f_s is 15kHz. The control board was connected directly to the driver without any interface. The SEMITOP® was fixed onto the heat sink using the correct thermal paste, as specified in the SEMITOP® mounting instructions (PI_19-00).

4.2. Delay time

The delay time introduced by the driver between the input logic signal and the V_{GE} signal applied at the IGBT gate should be kept as short as possible. In fact, a long delay time can affect the entire system, compromising overall system efficiency. Furthermore, the delay time between input logic and V_{GE} is often responsible for the poor response of the dynamic feedback, which limits the performance of the customer's application substantially. In the proposed demo board the total delay time is 220ns, which can be further improved if there is no need for an input logic interface.

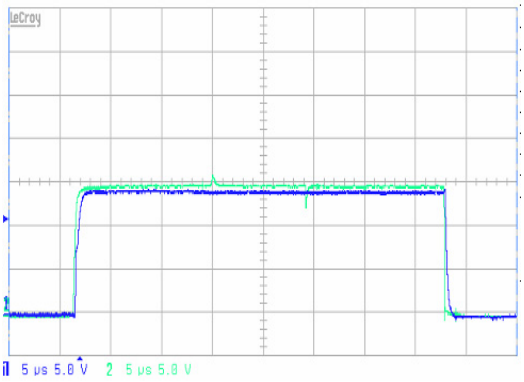


Figure 8: Input logic vs. V_{GE} output signals

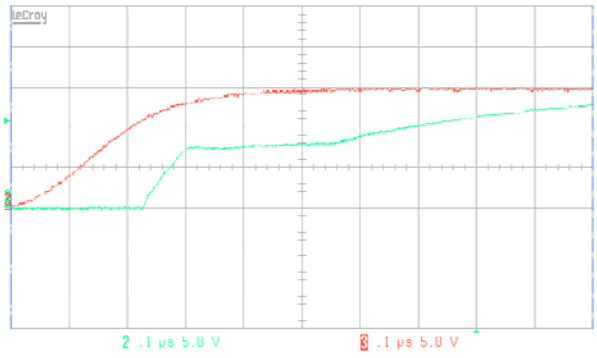


Figure 9: Zoomed view of input vs. output signals

4.3. Blanking time

The introduction of a blanking time between top and bottom input signals is necessary to avoid any cross-conduction due to the simultaneous commutation of the top and bottom switch of the same inverter leg. Fig. 10 shows the blanking time between top and bottom introduced by DSP. The blanking time value is around 600ns (see Fig. 10), which is enough to avoid undesired cross-conduction between the top and bottom IGBT of the same inverter leg.

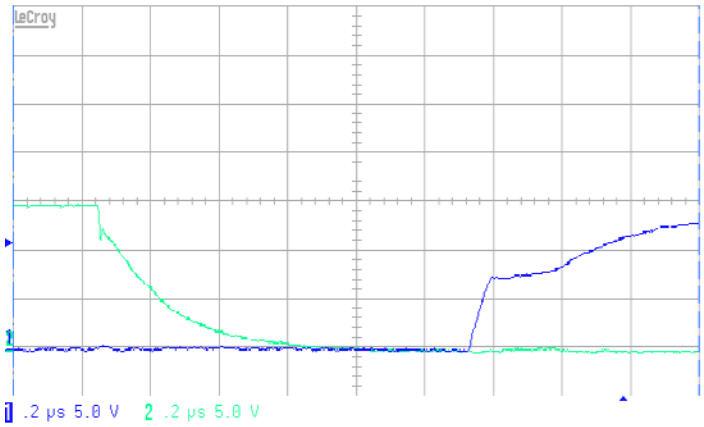


Figure10: Blanking time between top and bottom switch

4.4. Gate characteristics

Figs. 11 and 12 show the gate-to-emitter voltage and the gate current characteristics of the top and bottom IGBTs. From lab experience, the best performance in terms of switching energy losses can be achieved using two different gate resistances for turn-on and turn-off.
In the demo board R_{Gon} is 22Ω and R_{Goff} is 11Ω (see schematic in Fig. 2).

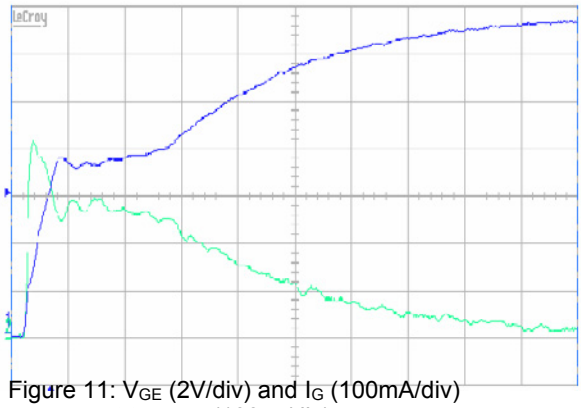


Figure 11: V_{GE} (2V/div) and I_G (100mA/div) at turn-on (100ns/div)

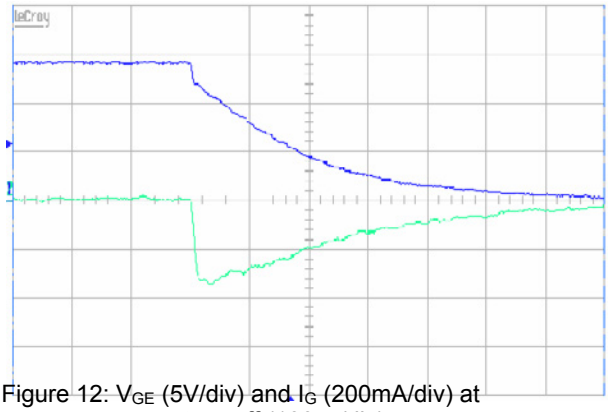


Figure 12: V_{GE} (5V/div) and I_G (200mA/div) at turn-off (100ns/div)

Even for a large-area IGBT chip (41mm^2), the positive peak current measured is around 400mA and the negative peak current around 350mA. Both these values are lower than those recommended by the ASIC manufacturer. This shows that the operating working conditions are not critical even if wider IGBT areas are being driven.

4.5. Switching characteristics

Fig. 13 and Fig. 14 show the V_{CE} and V_{GE} characteristics for top and bottom switches in full current conduction.

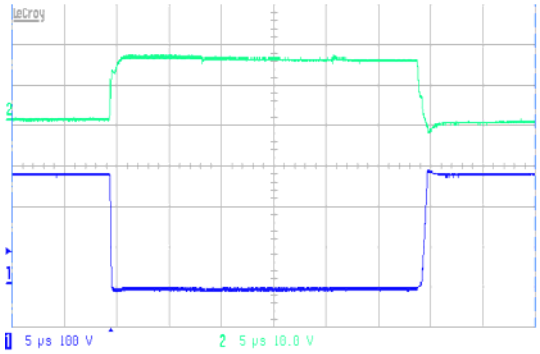


Figure 13: V_{CE} (100V/div) and V_{GE} (10V/div) of the top switch

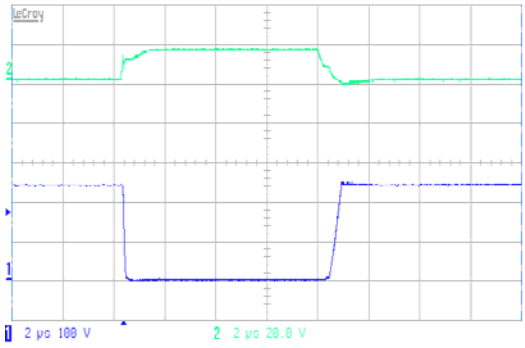


Figure 14: V_{CE} (100V/div) and V_{GE} (20V/div) of the bottom switch

In order to obtain these waveforms, particular attention was given to the PCB layout design. The ground traces were designed as wide and as short as possible. This led to a substantial reduction in the parasitic inductances (which are directly proportional to the trace length and inversely proportional to the trace width), resulting in fewer over-voltage spikes, improved EMI immunity and better driver robustness. Furthermore, this solution improves the EMI performance because large copper areas are able to shield and dissipate spurious RF better than thinner traces.

Another important consideration has to be factored into the design and connection of the DC link capacitors: the DC link capacitor bank is not included in the driver demo board, but has to be connected externally. The dimensioning of the DC link capacitors should therefore be carefully performed with proper consideration to load level and load type. Moreover, the DC link should be achieved using fast capacitors with a low ESR value in parallel with electrolytic capacitors in order to improve the dynamic response of the capacitor bank. Finally, DC link capacitors should be

connected to the demo board via bus bar connection (or large wires) that is as short as possible and as close as possible to the DC power header or even directly soldered between the DC PIN of the SEMITOP® and the GND PIN of the power connector header.

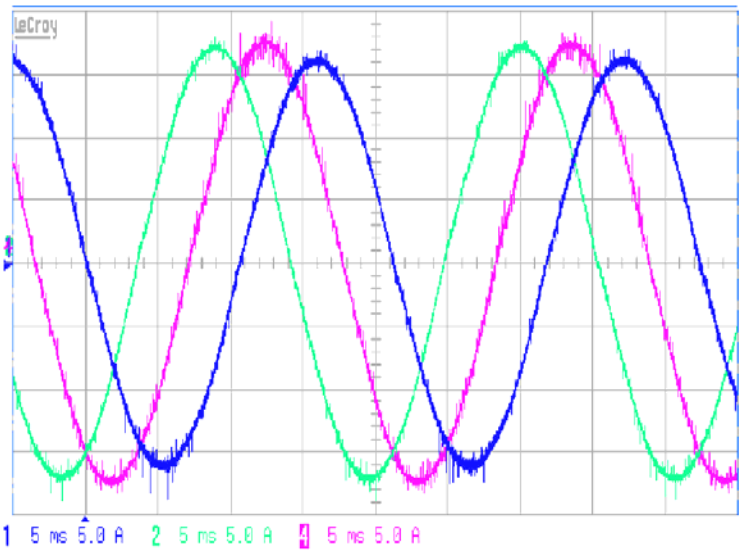
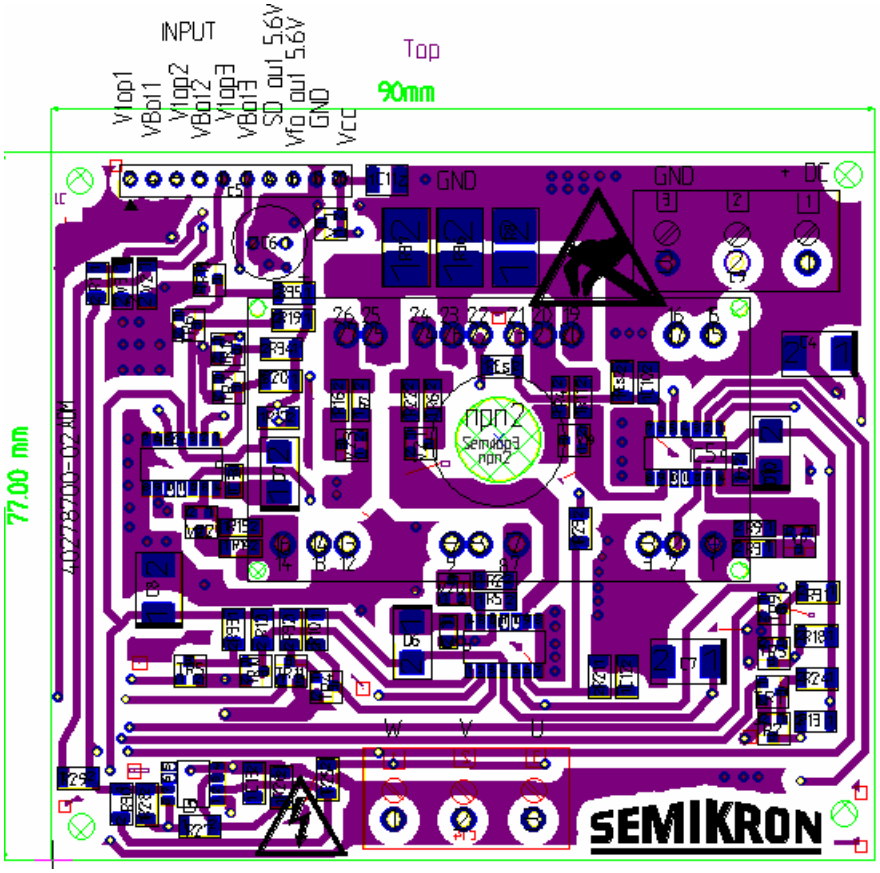


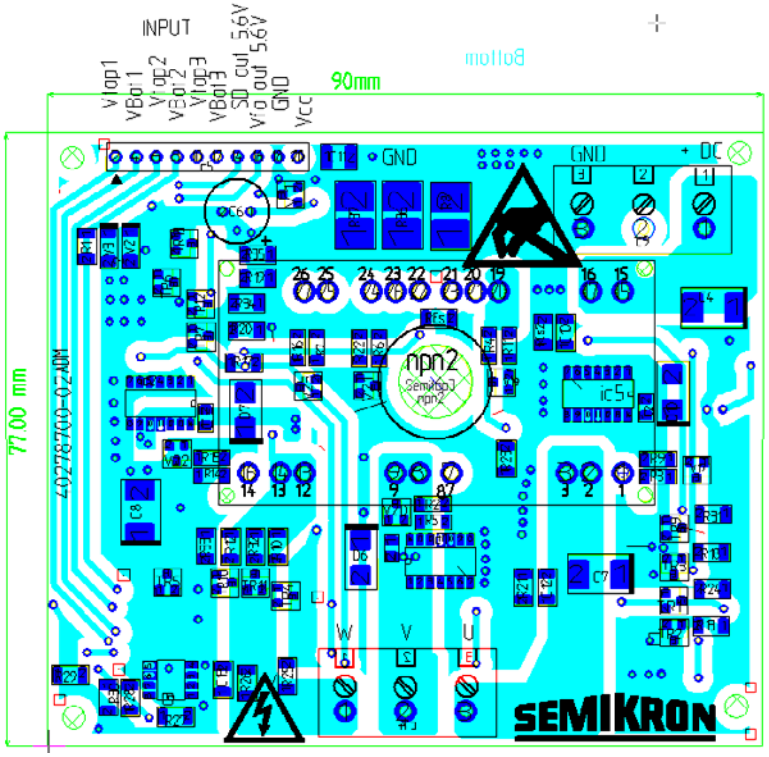
Figure 15: Line voltage and currents of 3-Ø induction motor load.

Demo board layout

Fig. 17 shows the layout (top and bottom layers on the left and right, respectively) of the demo board used for internal tests.



(a)



(b)

Figure 17: Demo board PCB layout; (a) top side and (b) bottom side.

Safety warning

Due to the fact that high voltages could be present on non-insulated parts, maximum care must be taken to prevent accidents. Remember there is no galvanic insulation between the high-voltage section and the logic section. Please consider that protection is not mandatory for application. SEMIKRON does not accept any responsibility for any accident caused by the incorrect /use or handling of parts and/or devices. The board may be operated by skilled personnel only.

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