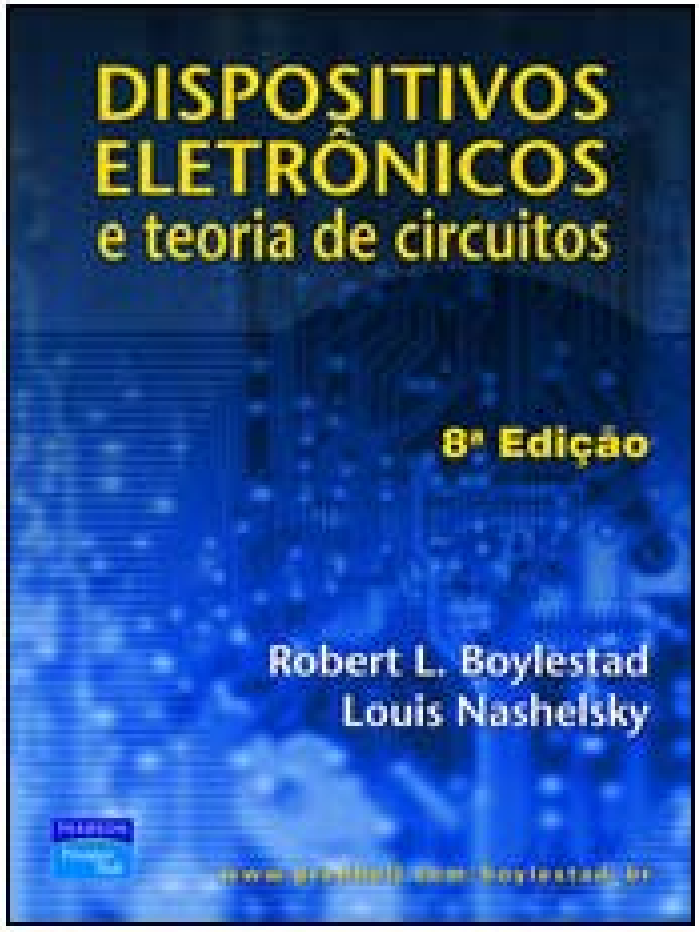
Universidade Federal de Santa Catarina
Departamento de Engenharia Elétrica
Materiais Elétricos - Laboratório

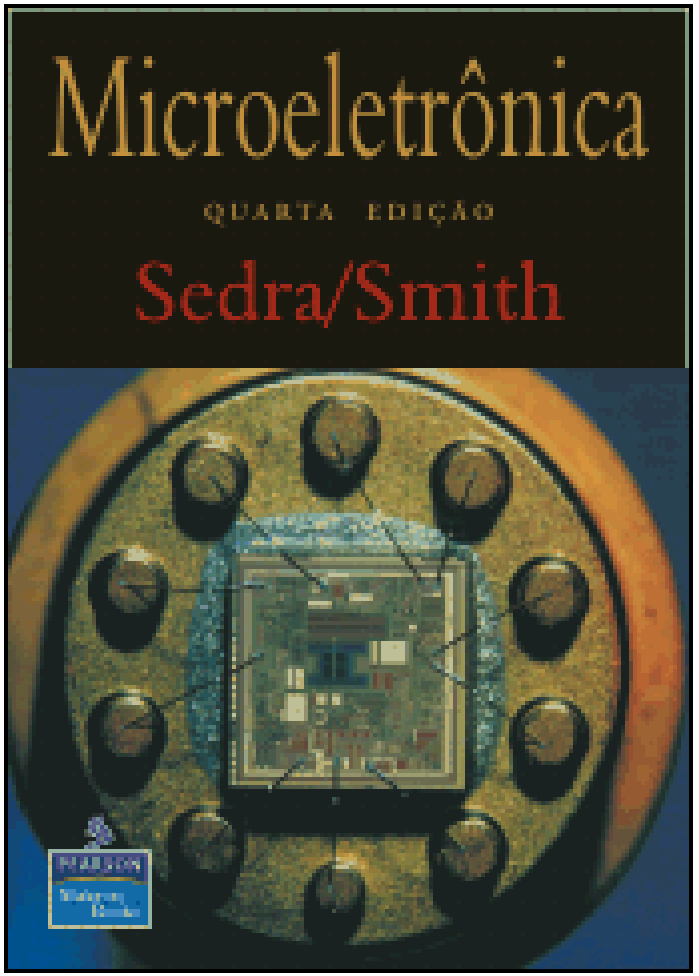
Curvas Características de Transistores e Portas Lógicas

Clóvis Antônio Petry, professor.

Florianópolis, agosto de 2006.

Semicondutores – referências bibliográficas





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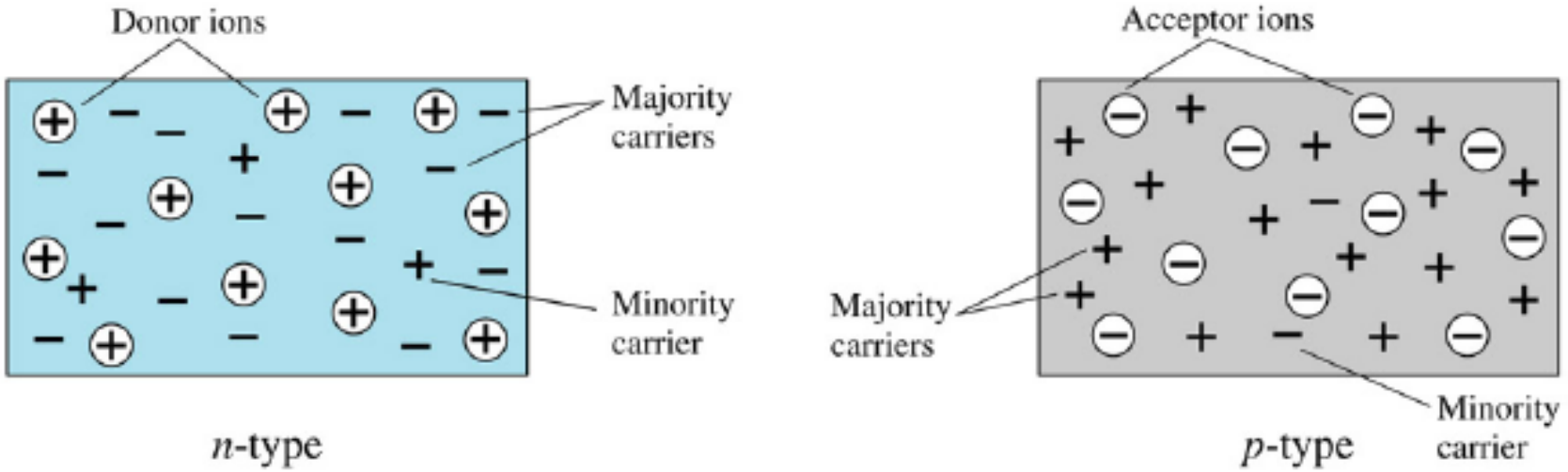
Semicondutores – materiais P e N



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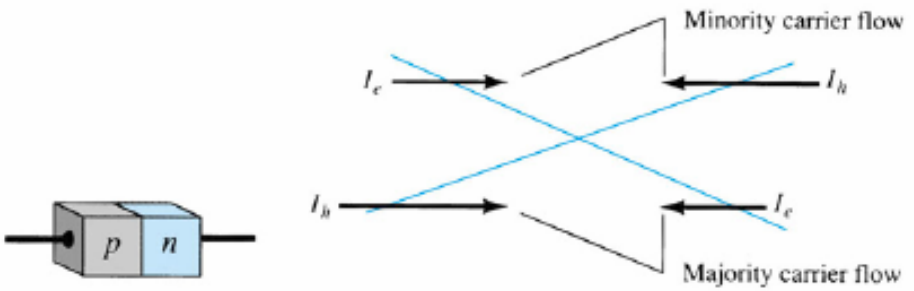

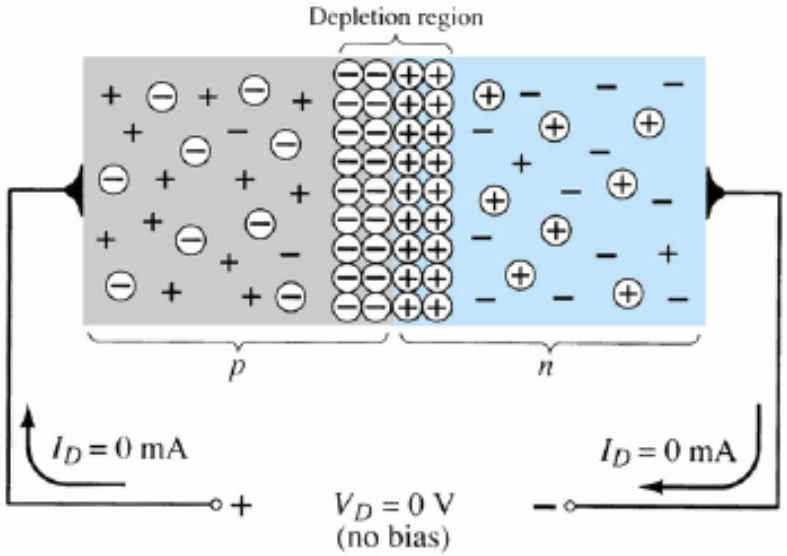

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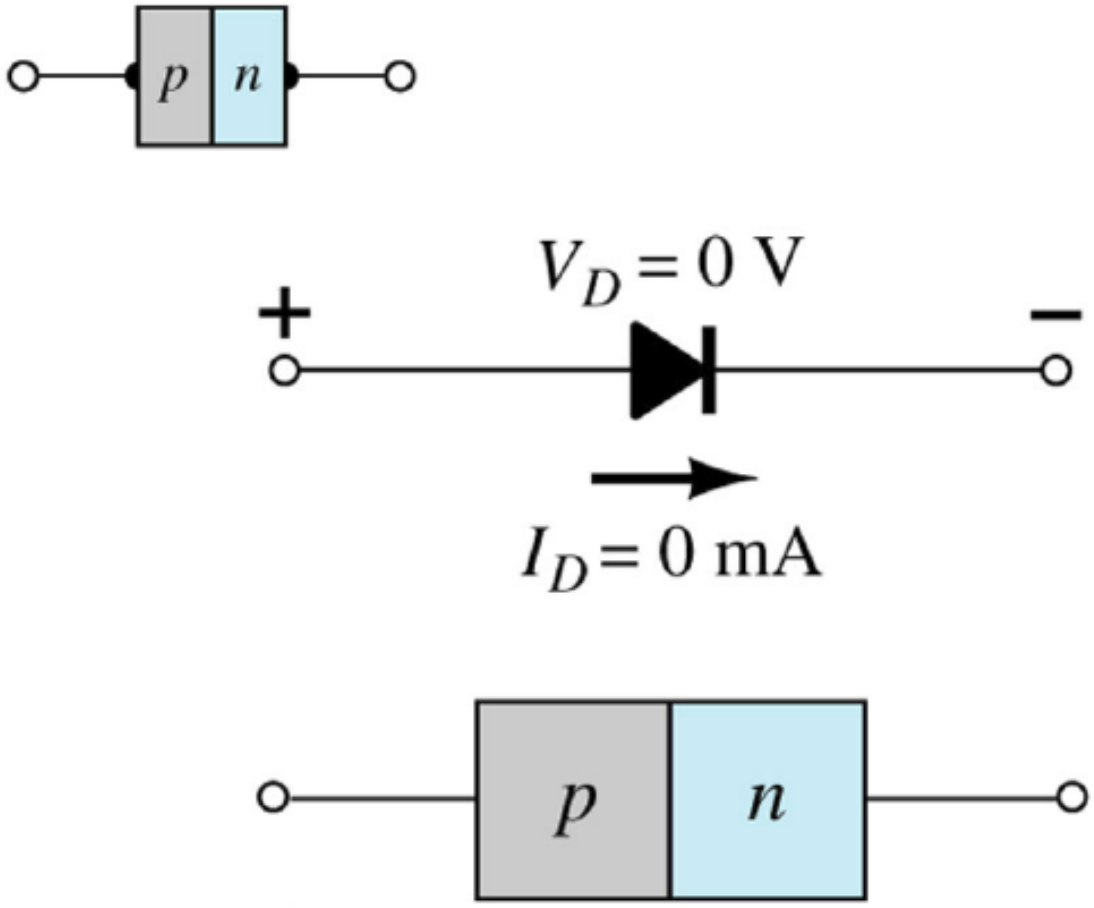

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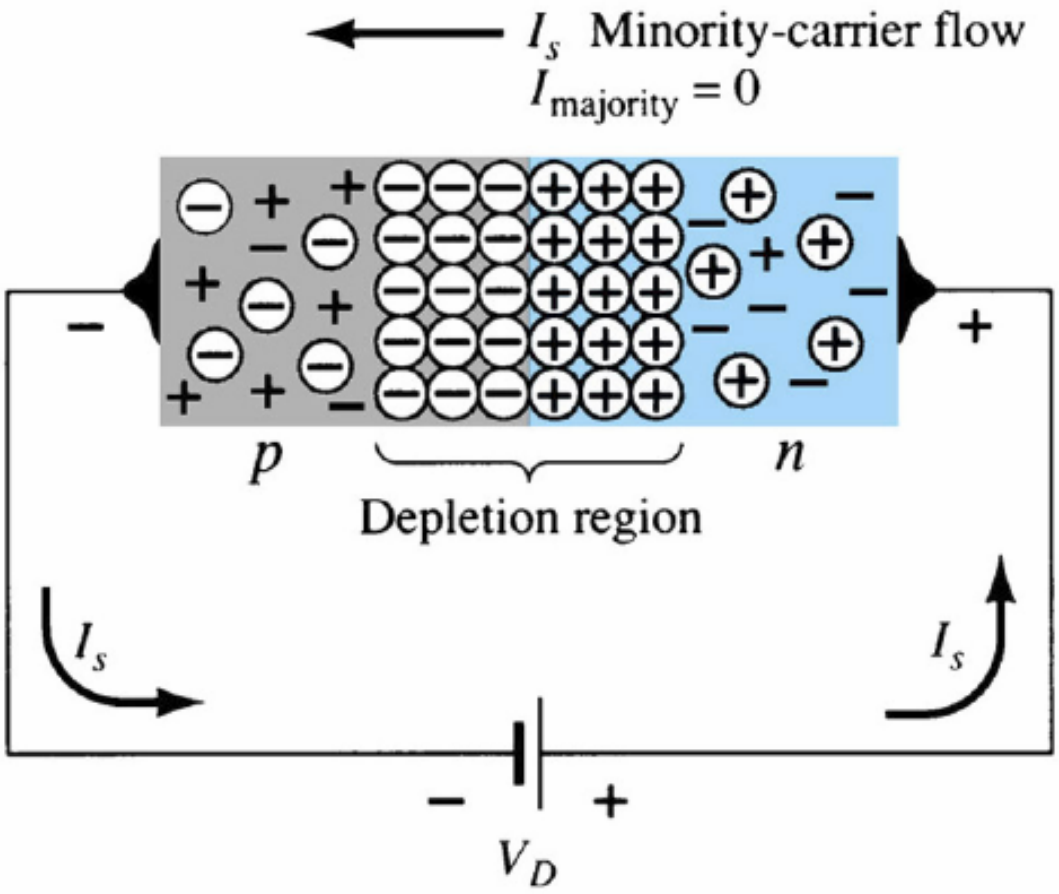

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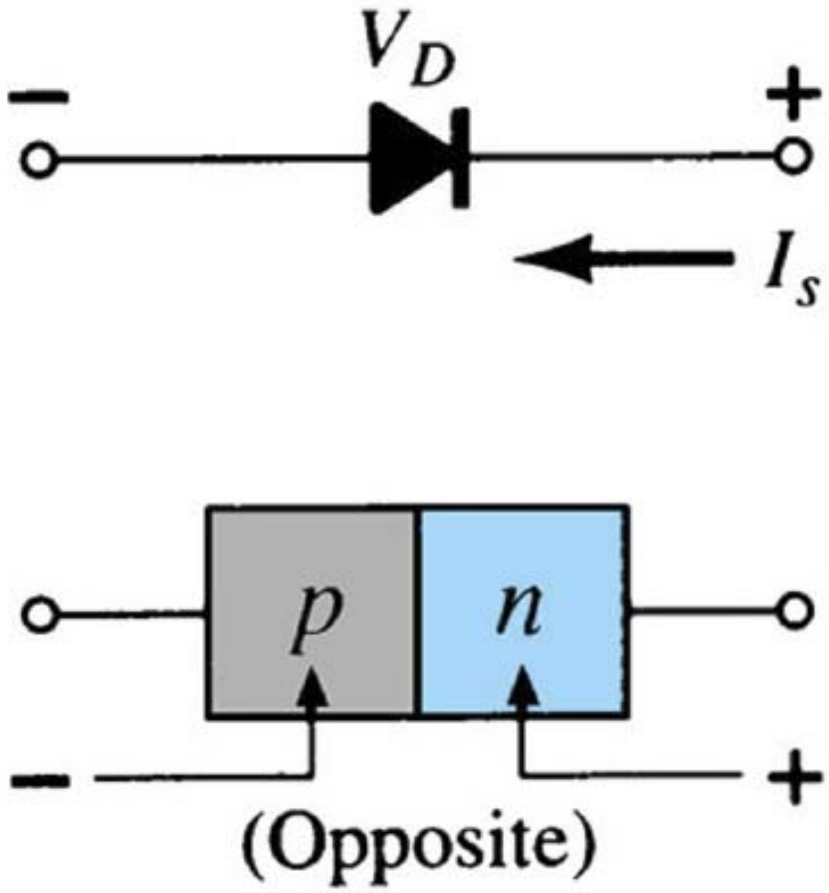

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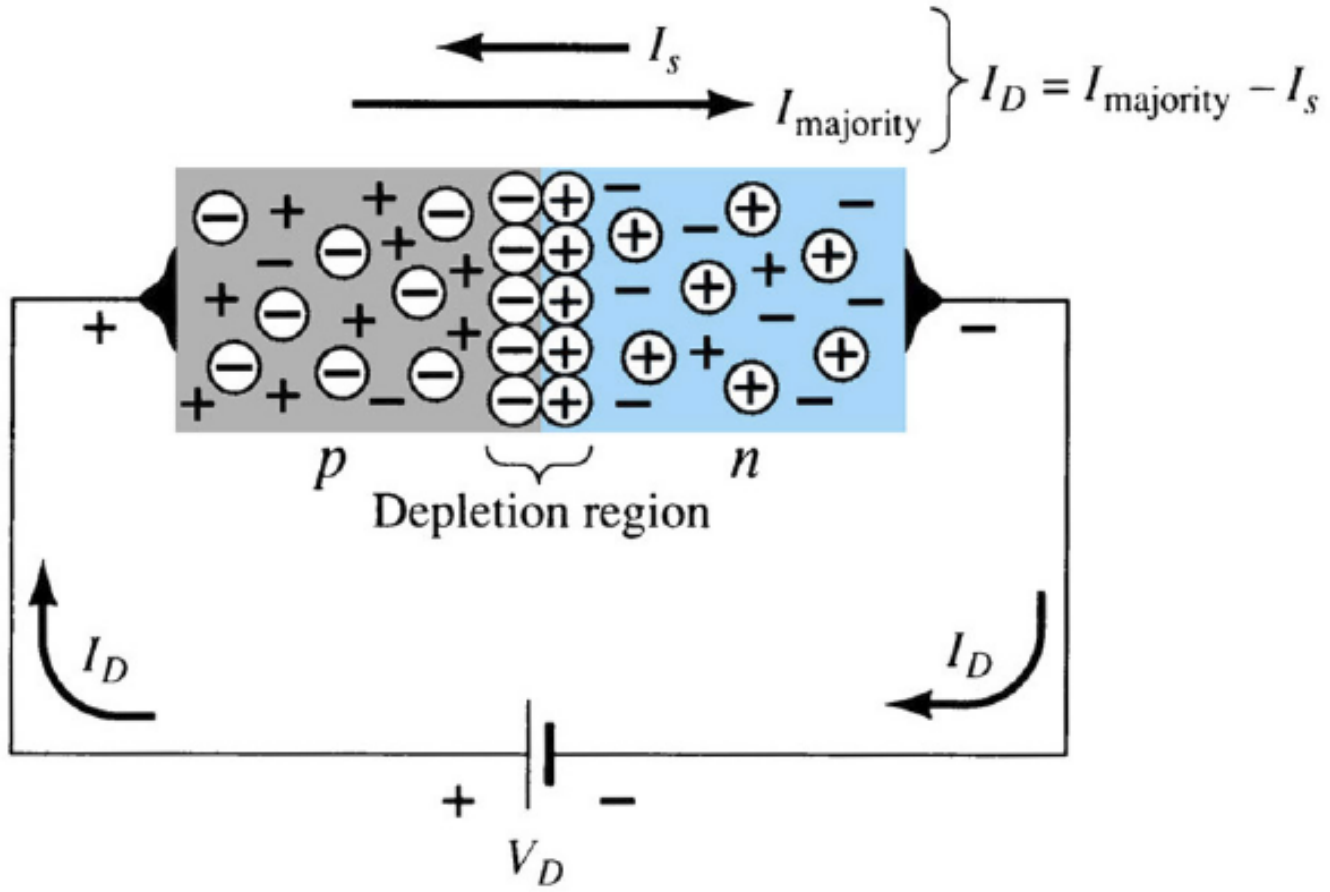
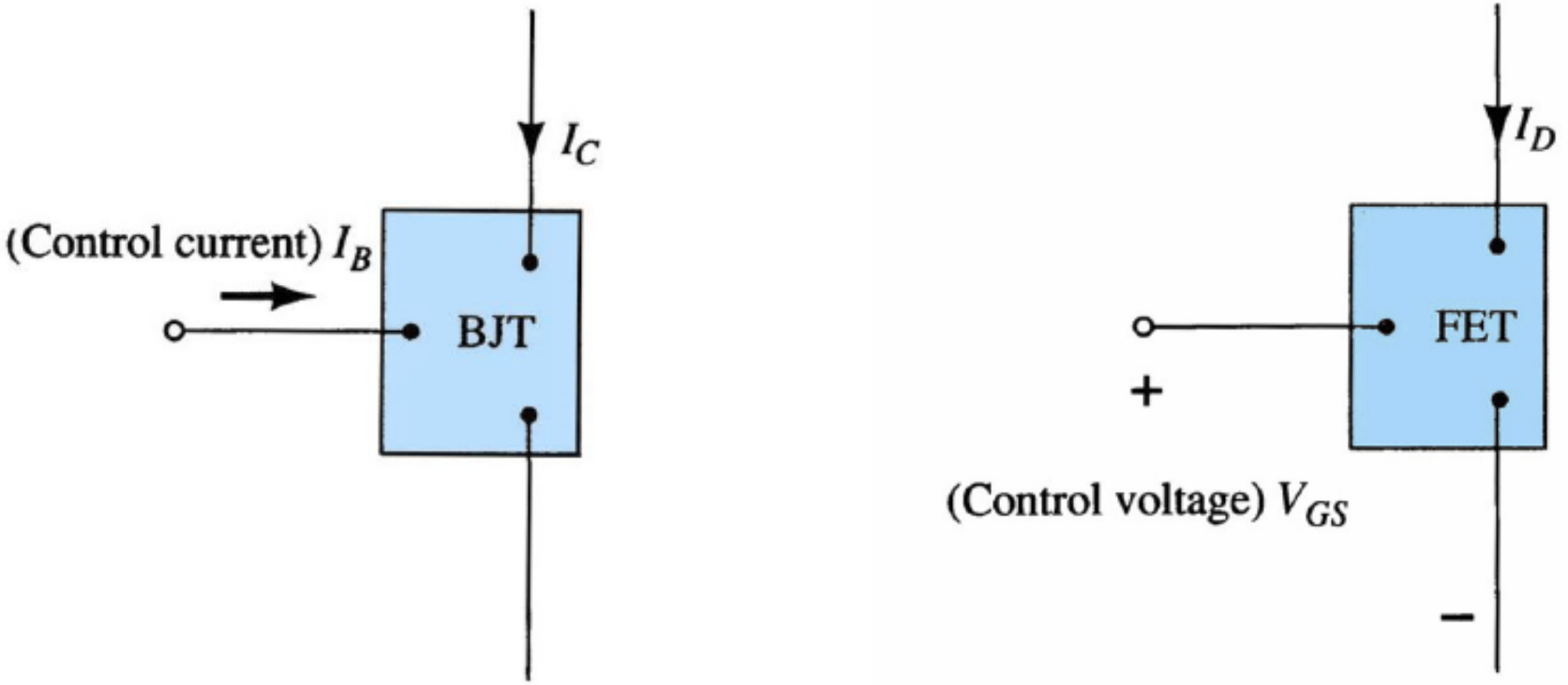
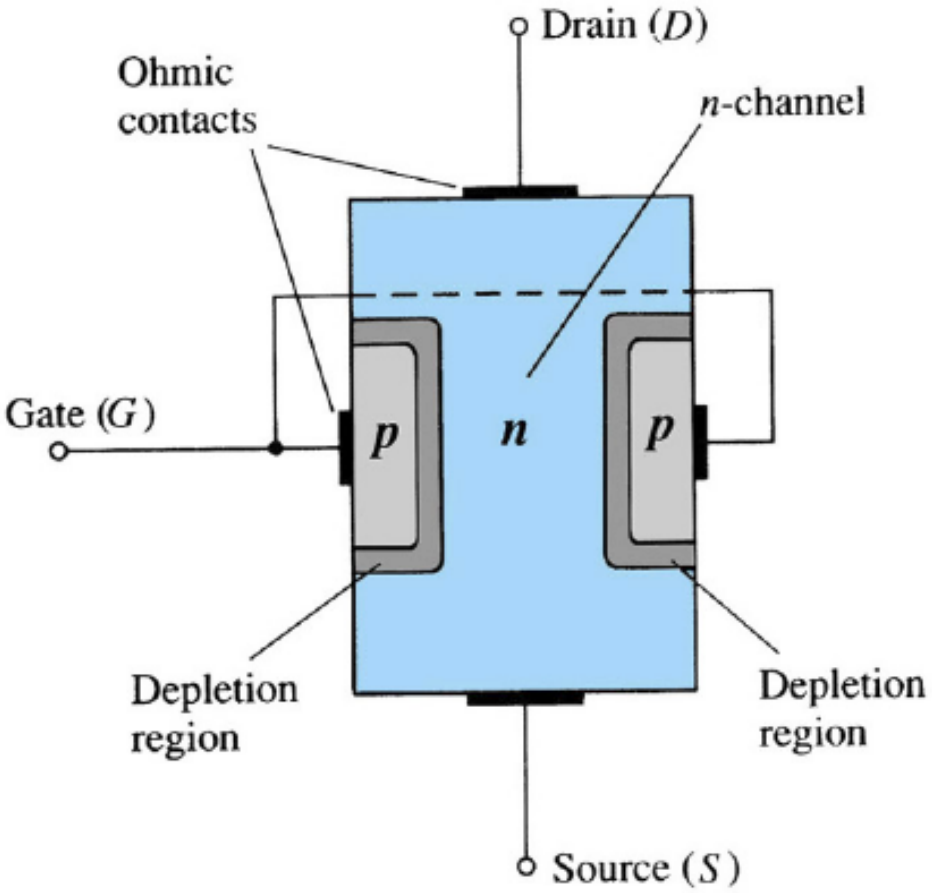
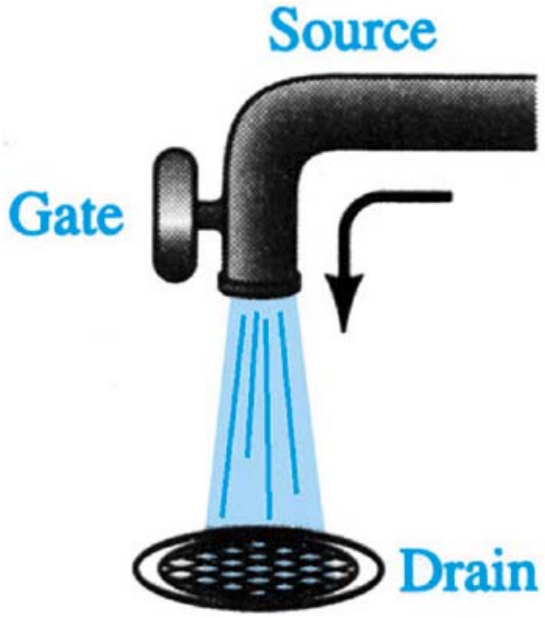


Transistor de efeito de campo

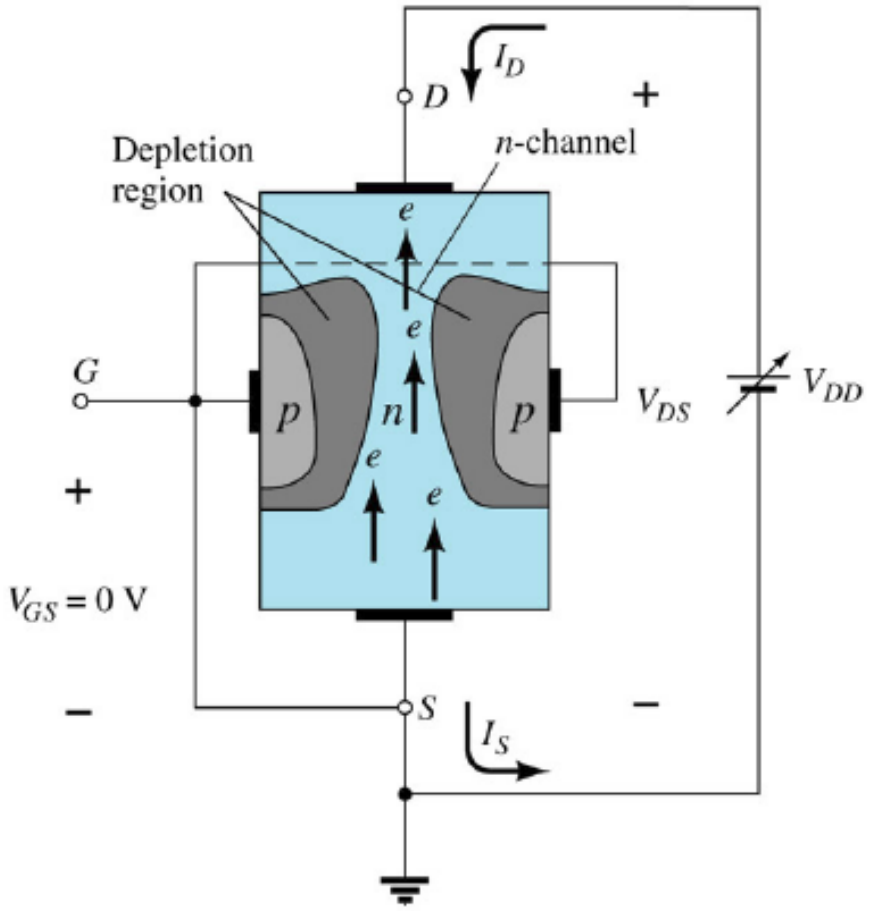


JFET – Estrutura interna





JFET - Funcionamento



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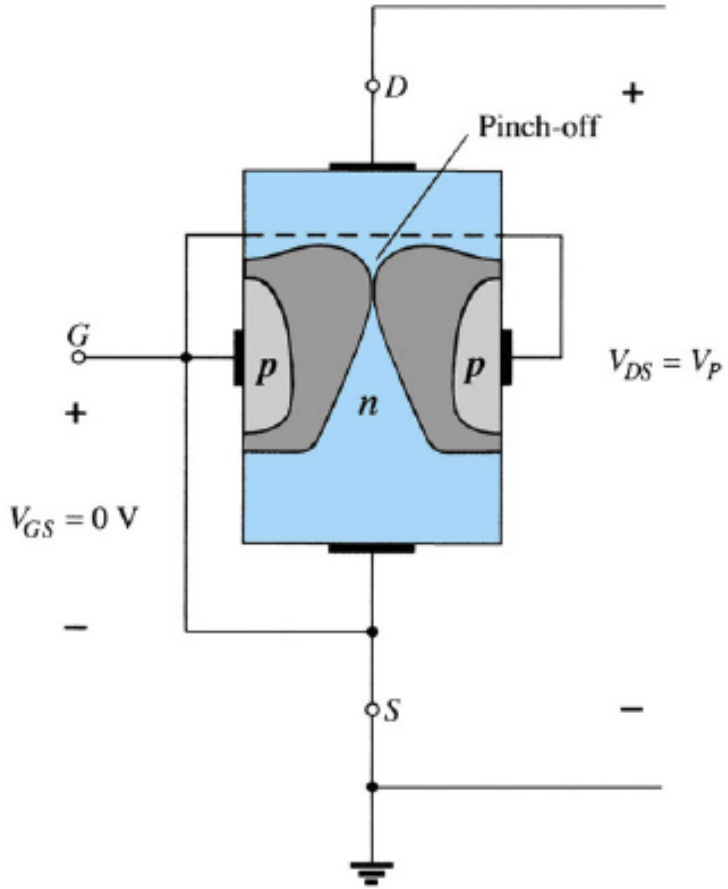

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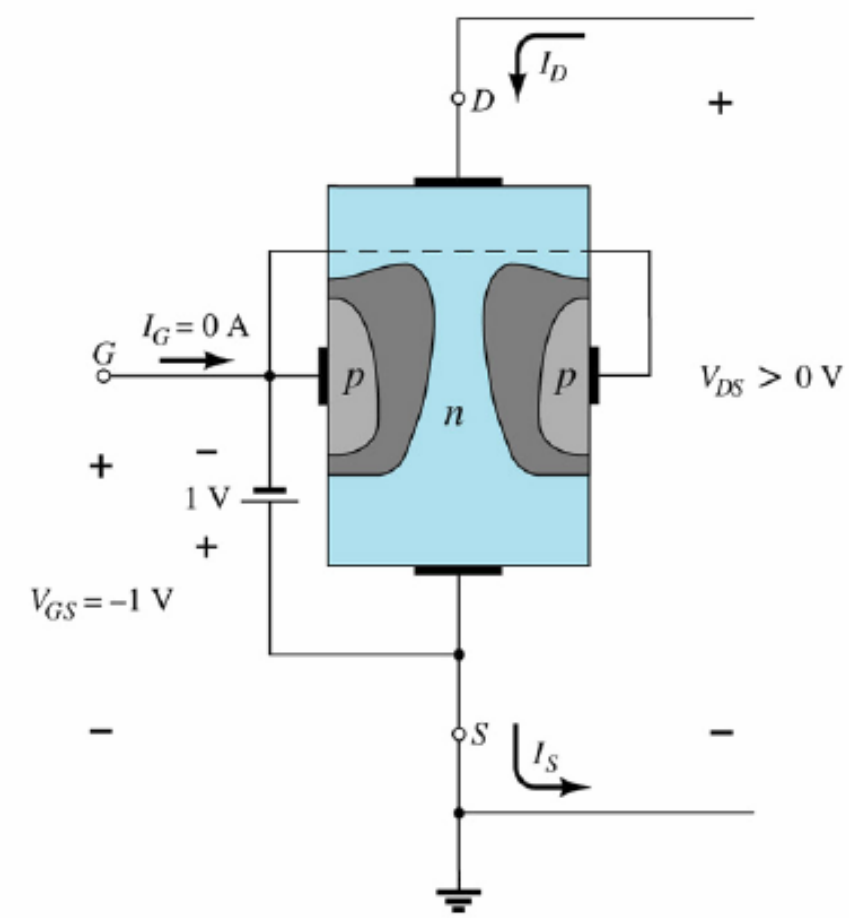
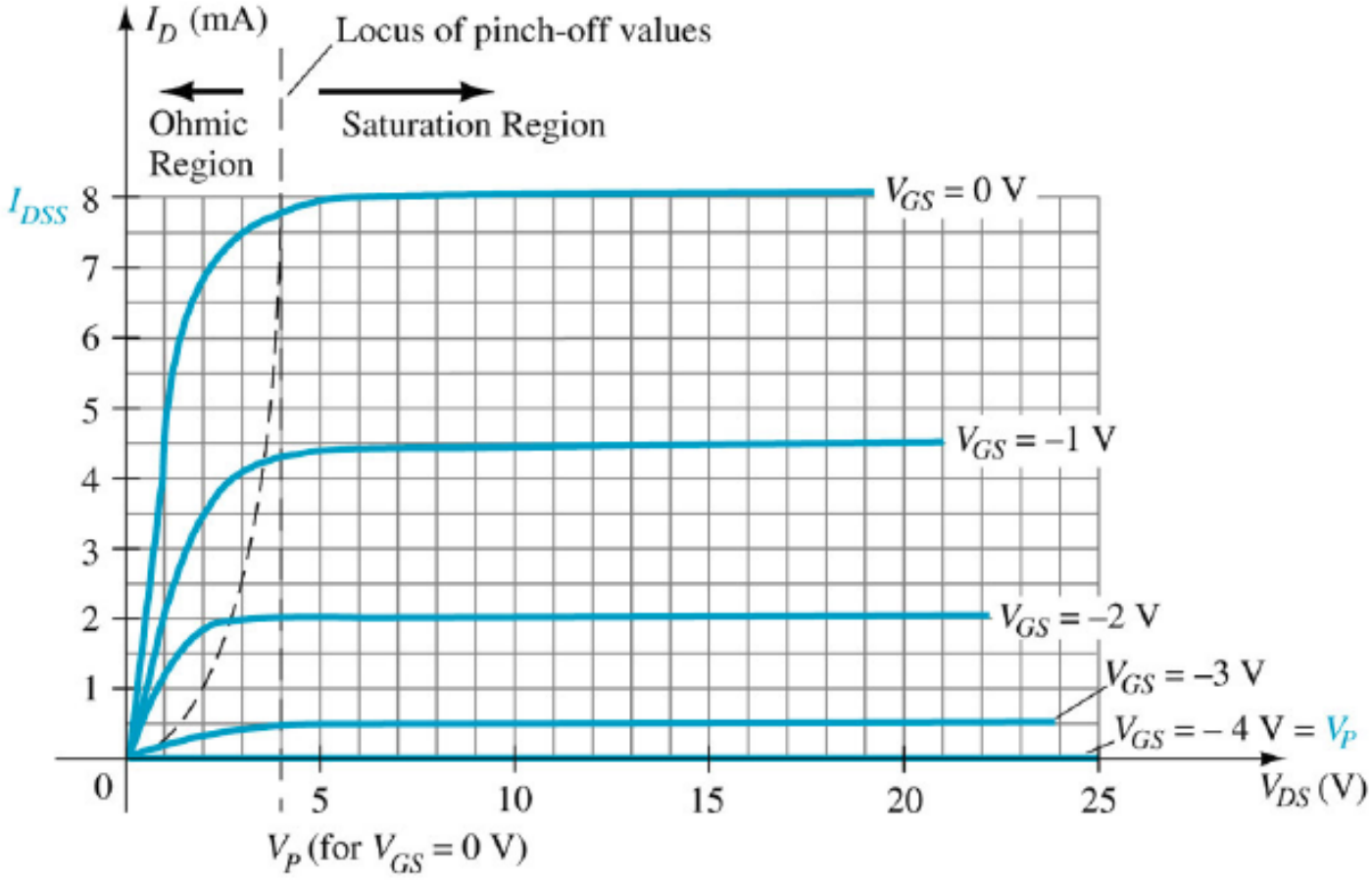
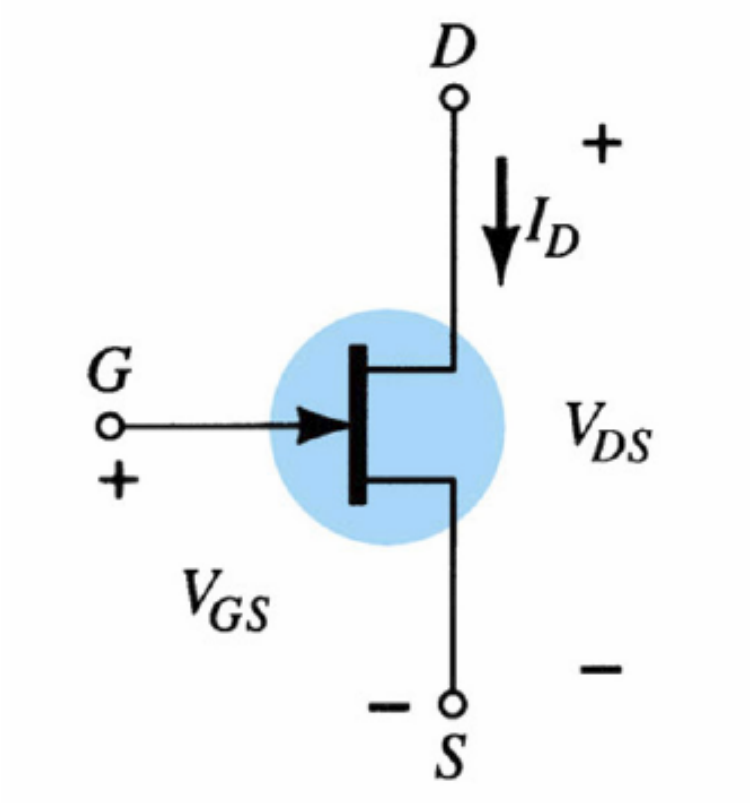


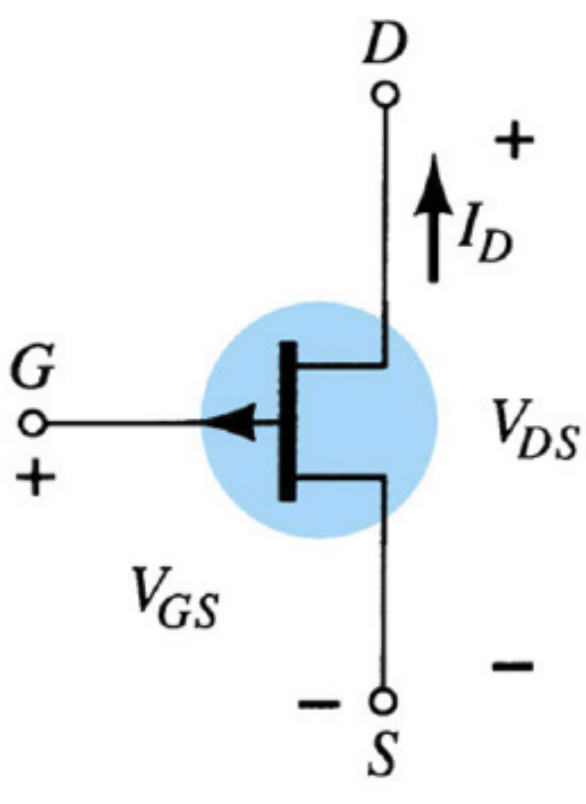
JFET – Curvas características



JFET - Simbologia

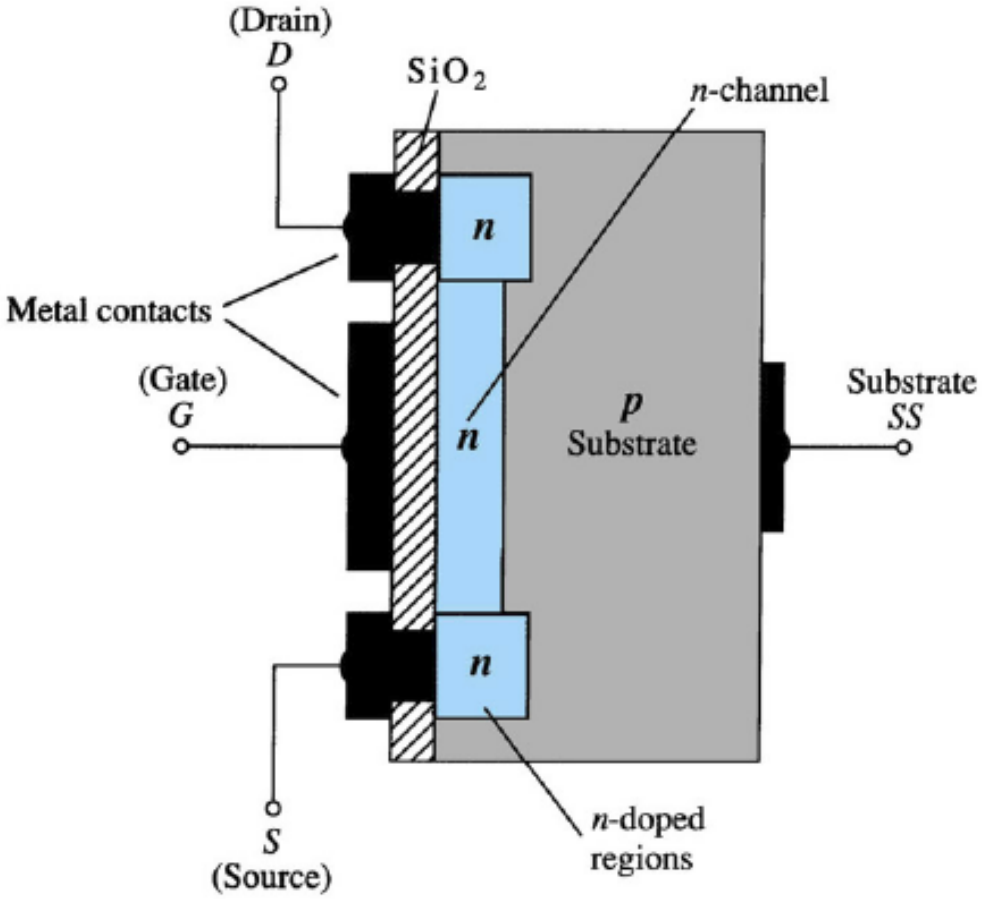


Canal N

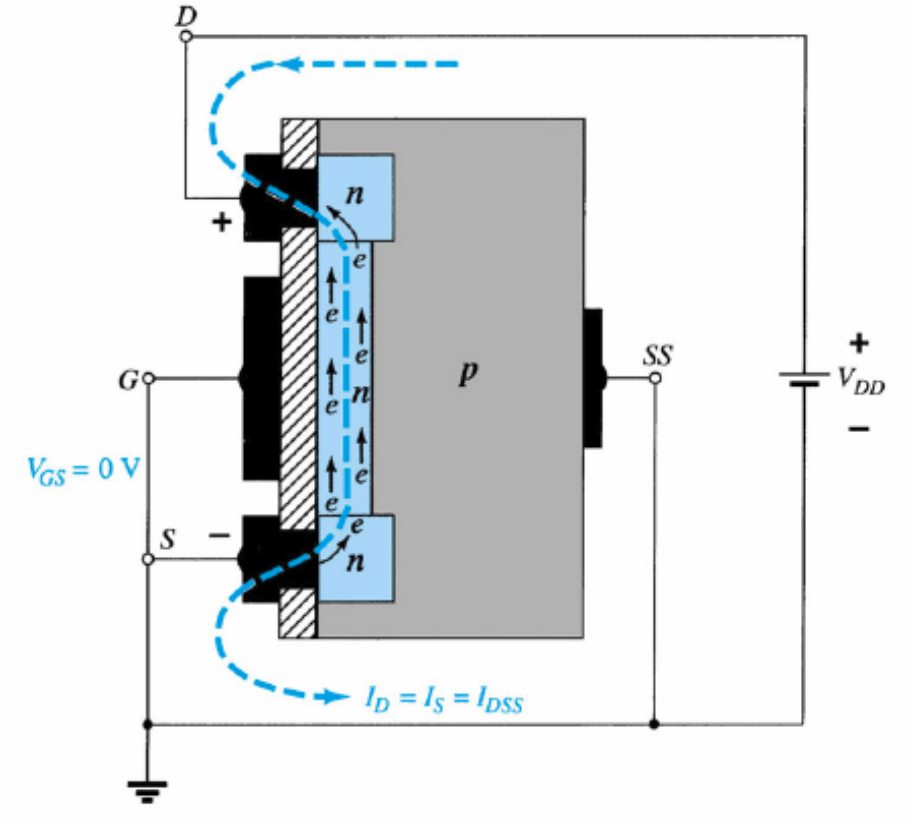


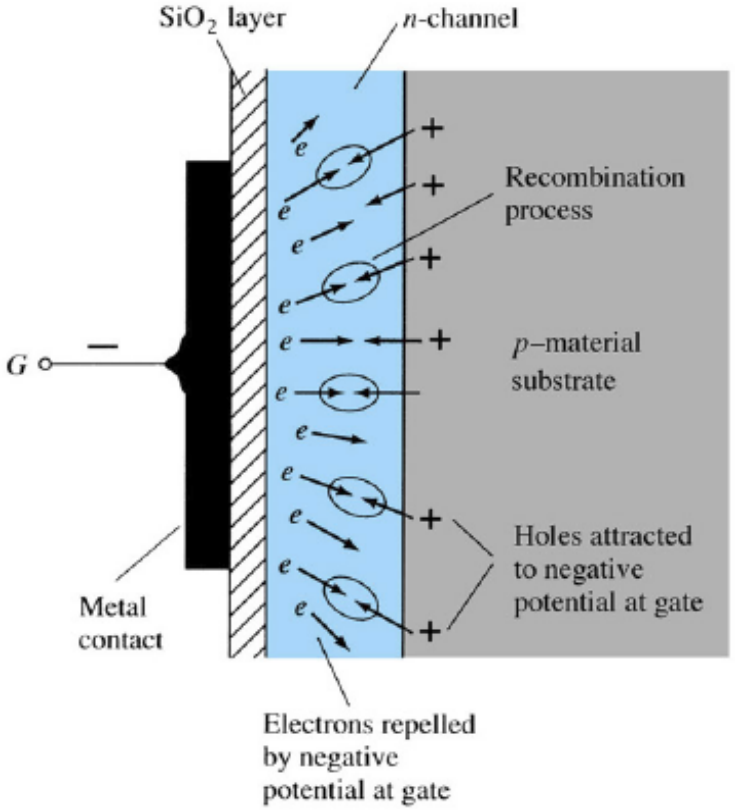
Canal P

MOSFET tipo depleção – Estrutura interna

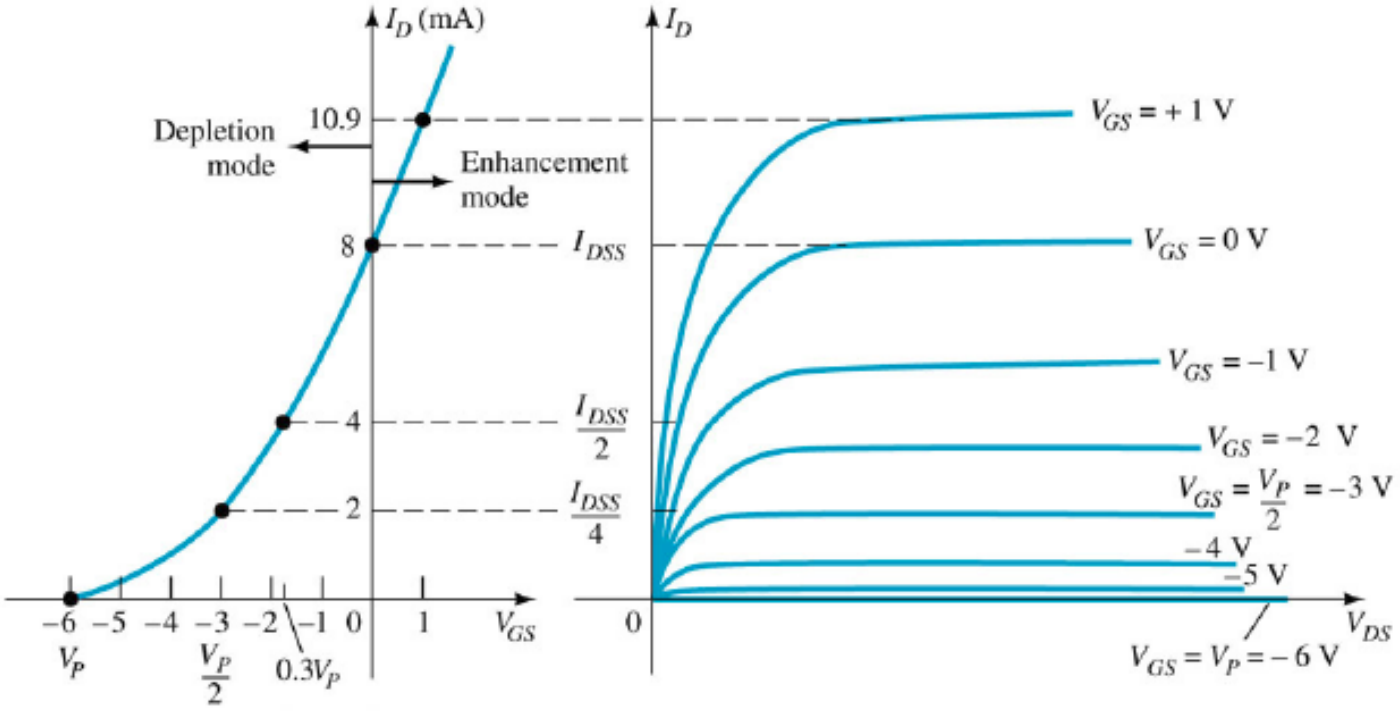


MOSFET tipo depleção - Funcionamento



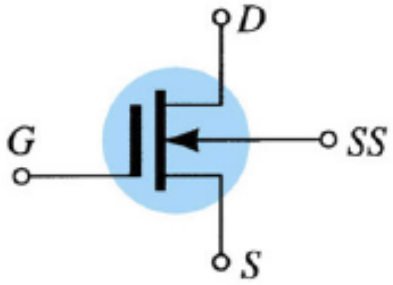


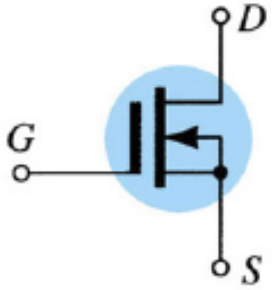
MOSFET tipo depleção – Curvas características



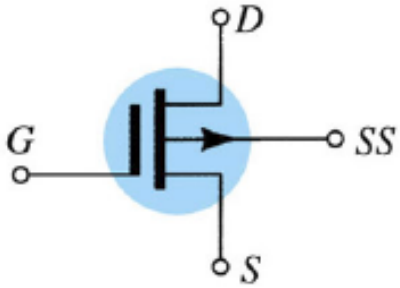
MOSFET tipo depleção - Simbologia

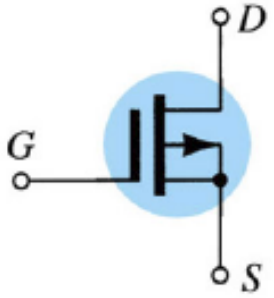
n-channel



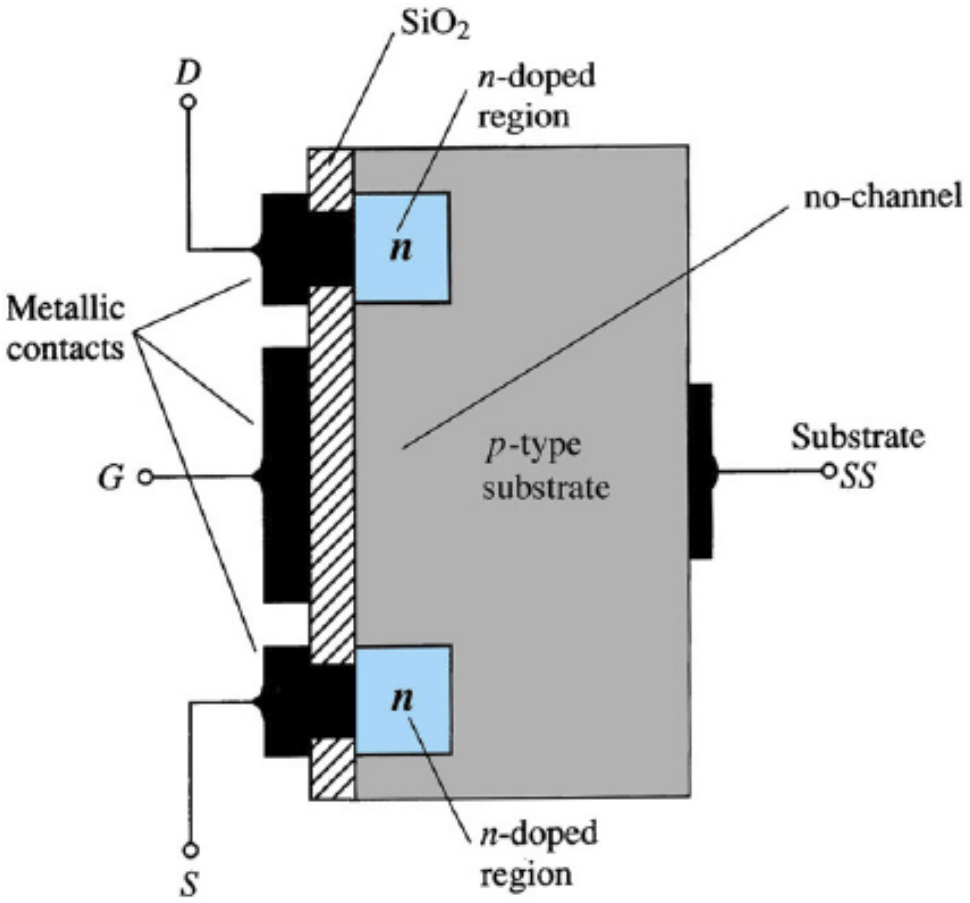


p-channel

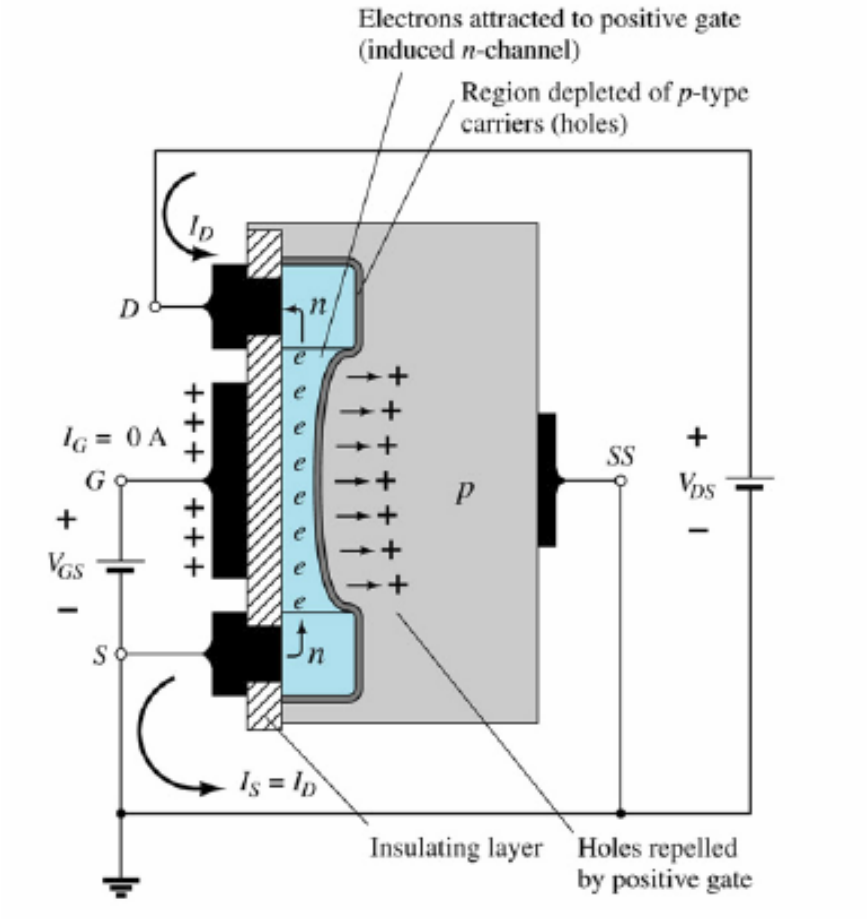




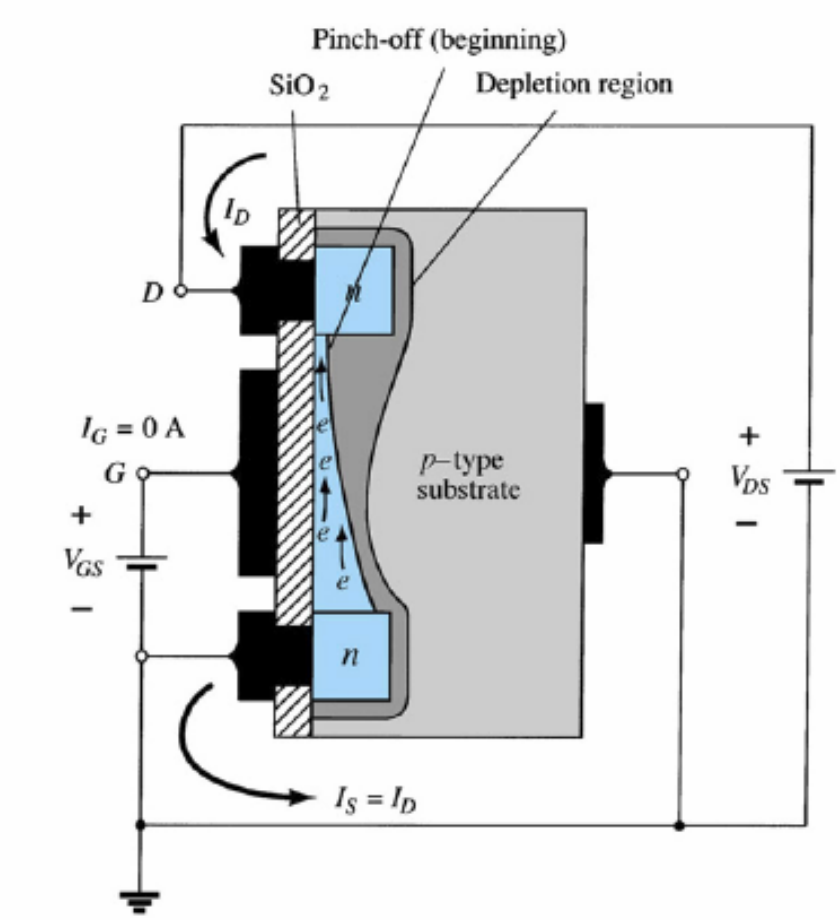
MOSFET tipo intensificação – Estrutura interna



MOSFET tipo intensificação – Funcionamento



MOSFET tipo intensificação – Funcionamento



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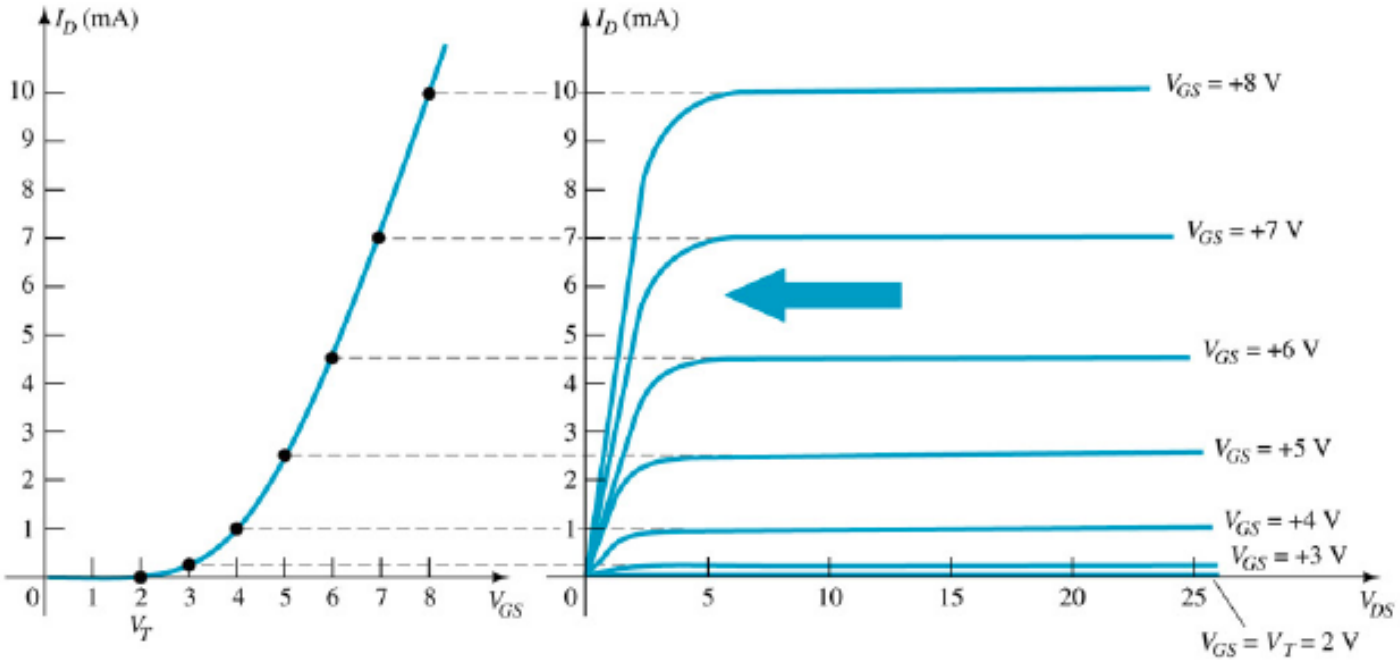


MOSFET tipo intensificação – Curvas caract.

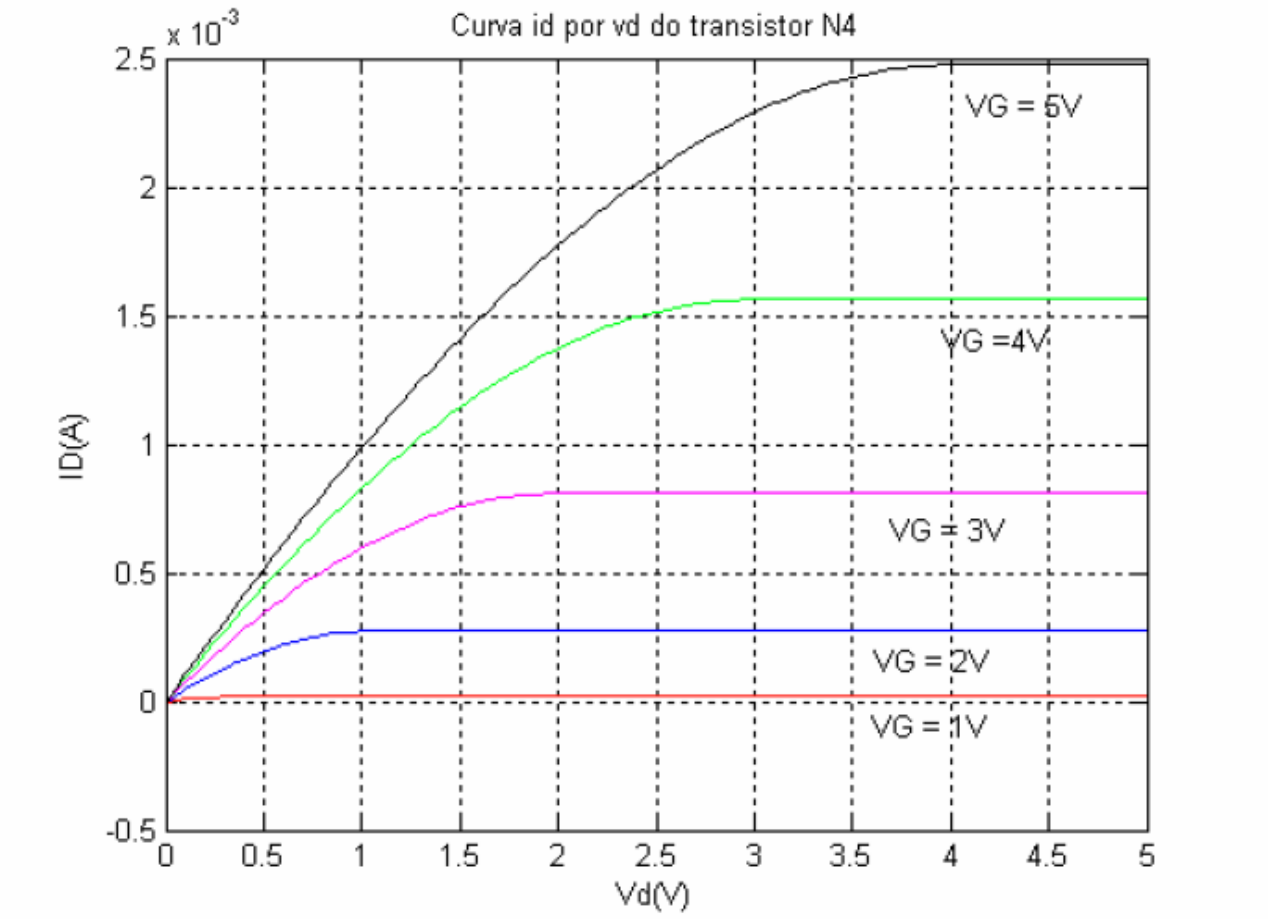
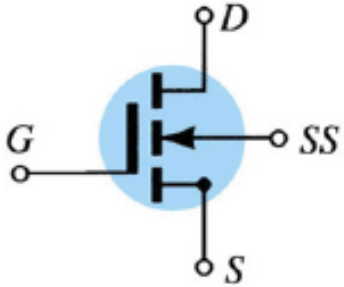


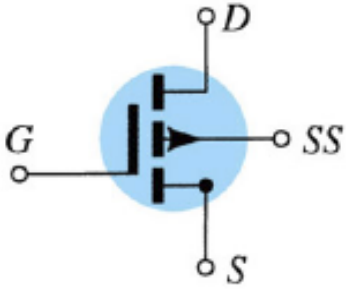
Figura 6 - Curvas I_D versus V_D em função de V_G para o transistor N_4 do chip didático.

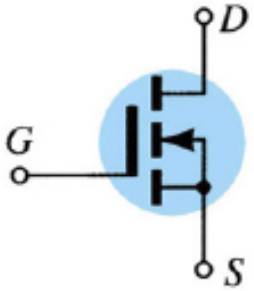
MOSFET tipo intensificação – Simbologia

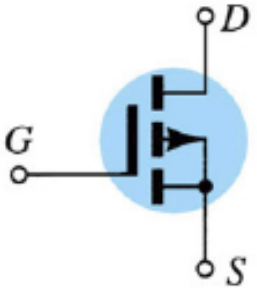
n-channel



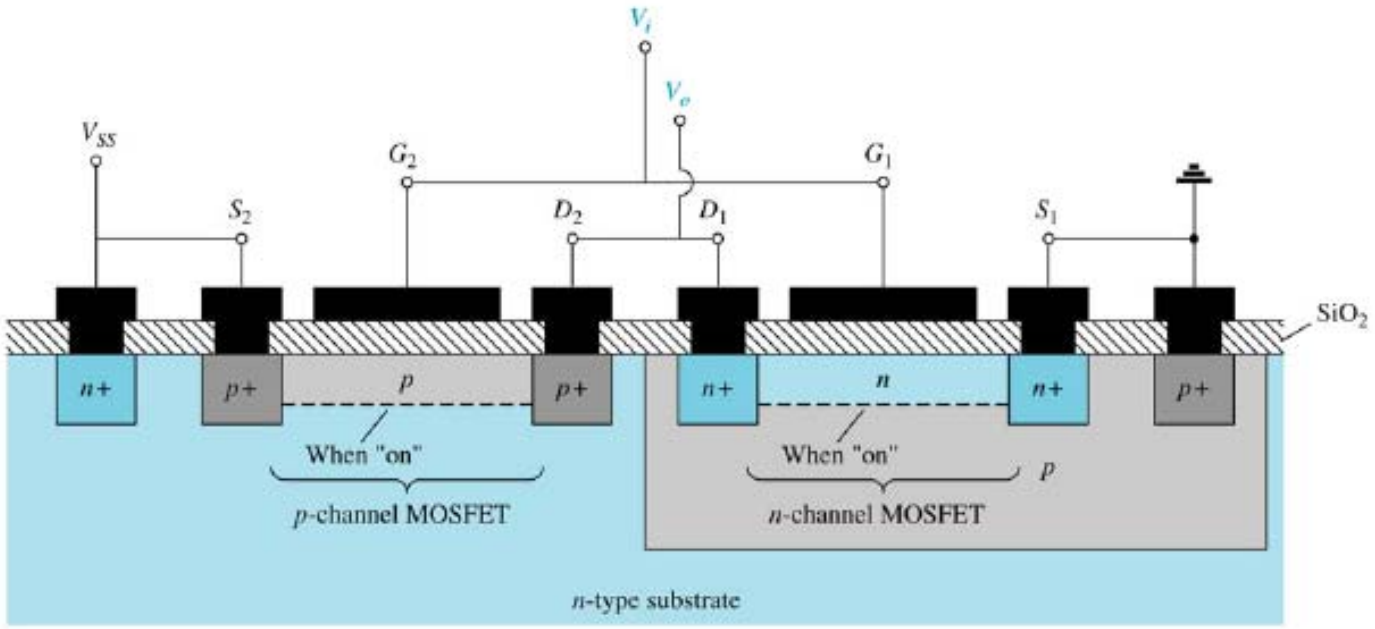
p-channel



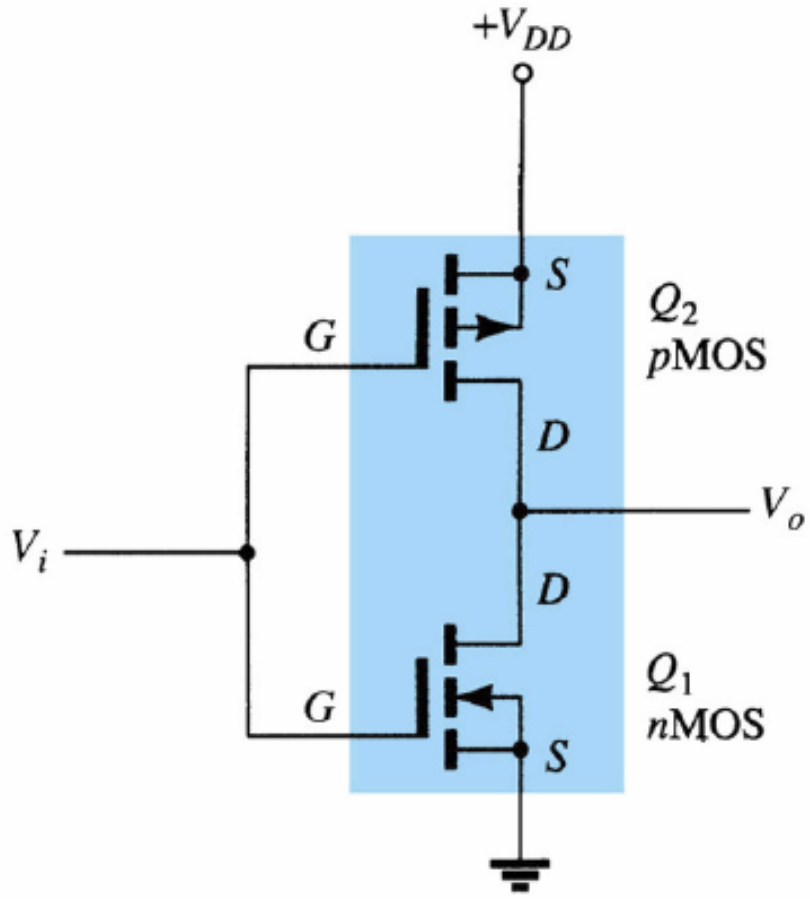




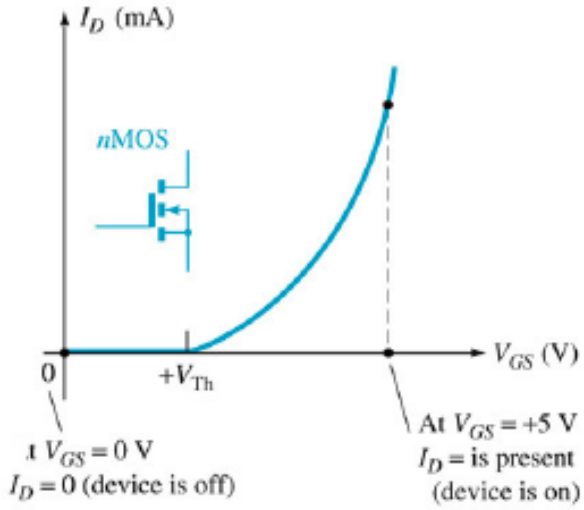
Inversor CMOS – Estrutura interna

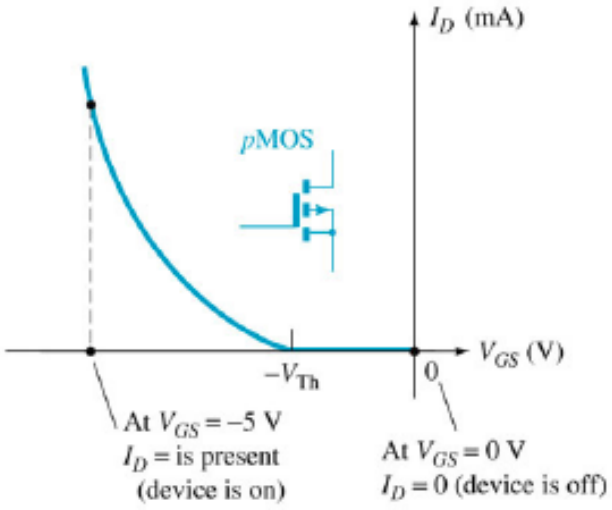


Inversor CMOS – Circuito elétrico

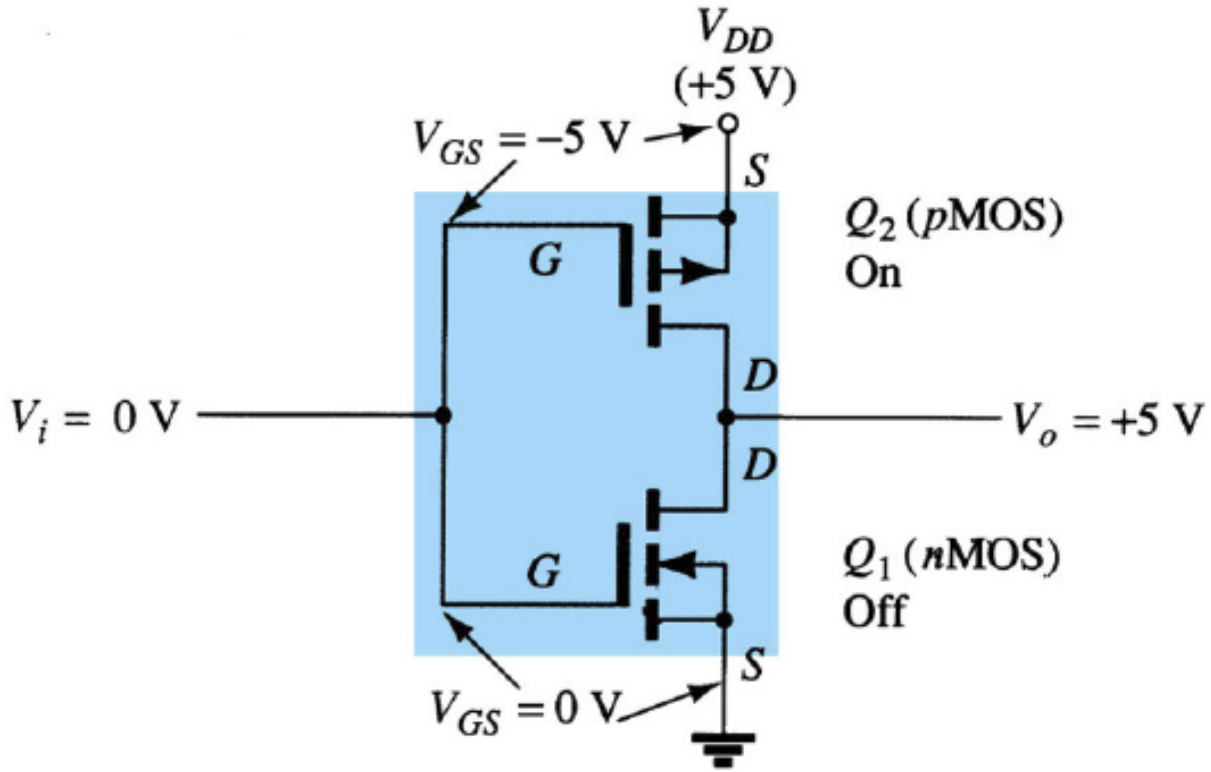


Inversor CMOS – Curvas dos transistores

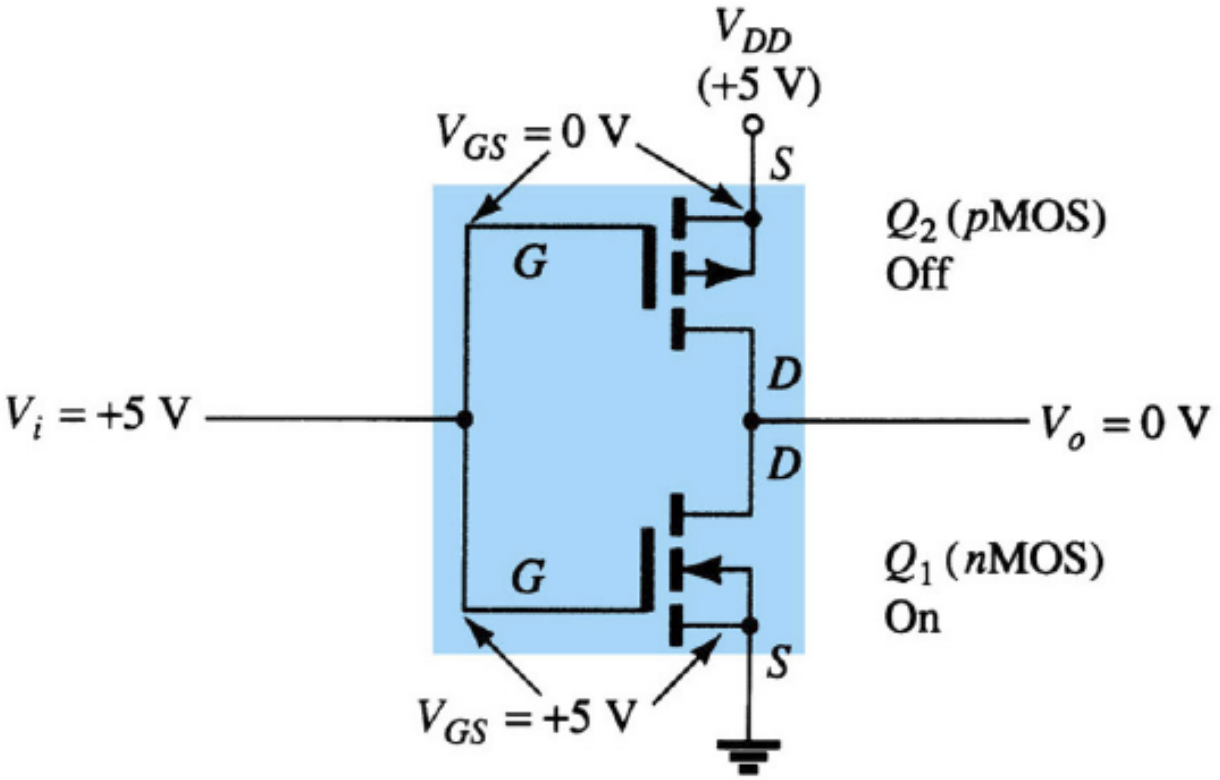




Inversor CMOS – Funcionamento



Inversor CMOS – Funcionamento



Circuito integrado didático

Pinagem e descrição dos terminais do CI.

Pinos	Descrição
1	Bulk N_2 e N_4
2	Source\drain N_2
3	Source\drain N_1
4	Bulk N_1
5	Source\drain N_1 e P_1
6	Source\drain P_1
7	Bulk P_1
8	Gate P_1 e N_1
9	Bulk P_2
10	Gate P_2 e N_2
11	Source\drain P_2
12	Source\drain P_2 e P_3
13	Source\drain P_3
14	Gate P_3 e N_3
15	Bulk P_3
16	Source\drain N_3 e N_2
17	Bulk N_3
18	Source\drain N_3 e N_4
19	Gate N_4 e P_4
20	Source\drain N_4 e P_4

Pinos	Descrição
21	Bulk P_4
22	Centro superior R_{sp}
23	Canto superior R_{sp}
24	Centro Lateral esquerda R_{sp}
25	Canto inferior esquerdo R_{sp}
26	Centro inferior R_{sp}
27	Contato direito R_{sp}
28	R_6 resistor serpentina (resistor de poço) 10 KΩ
29	R_6 resistor serpentina (resistor de poço) 10 KΩ
30	R_3 e R_1 (R_3 resistor de poço 4,7 KΩ)
31	R_1 (resistor de poly) 1 KΩ
32	R_2 (resistor de poly) 1 KΩ
33	Ground
34	V_{dd}
35	R_3 e R_2
36	R_4 (resistor de poly) 500 Ω
37	R_4 (resistor de poly) 500 Ω
38	R_8 (resistor de poly) 500 Ω
39	R_8 (resistor de poly) 500 Ω
40	Source\drain P_4

Circuito integrado didático

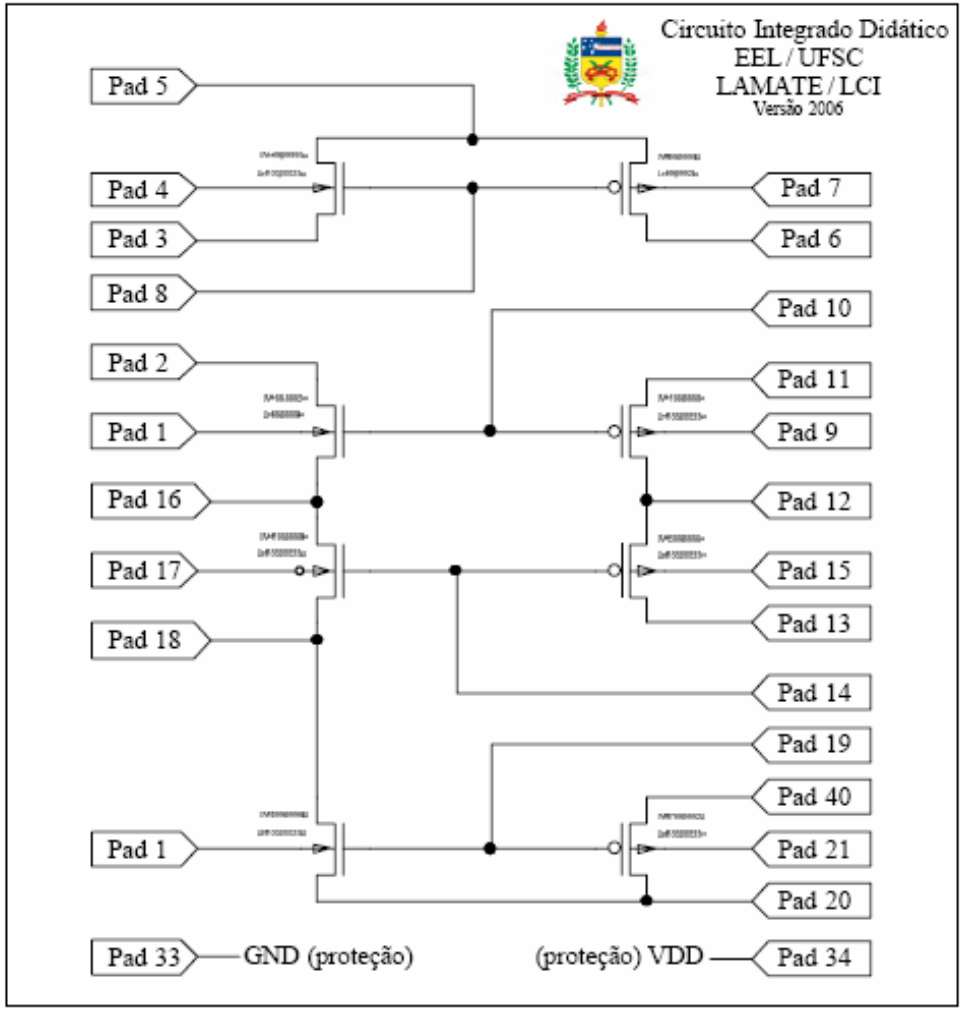


Figura 11 - Esquema de ligação interna do circuito integrado didático.

Parte Experimental – Curvas do NMOS

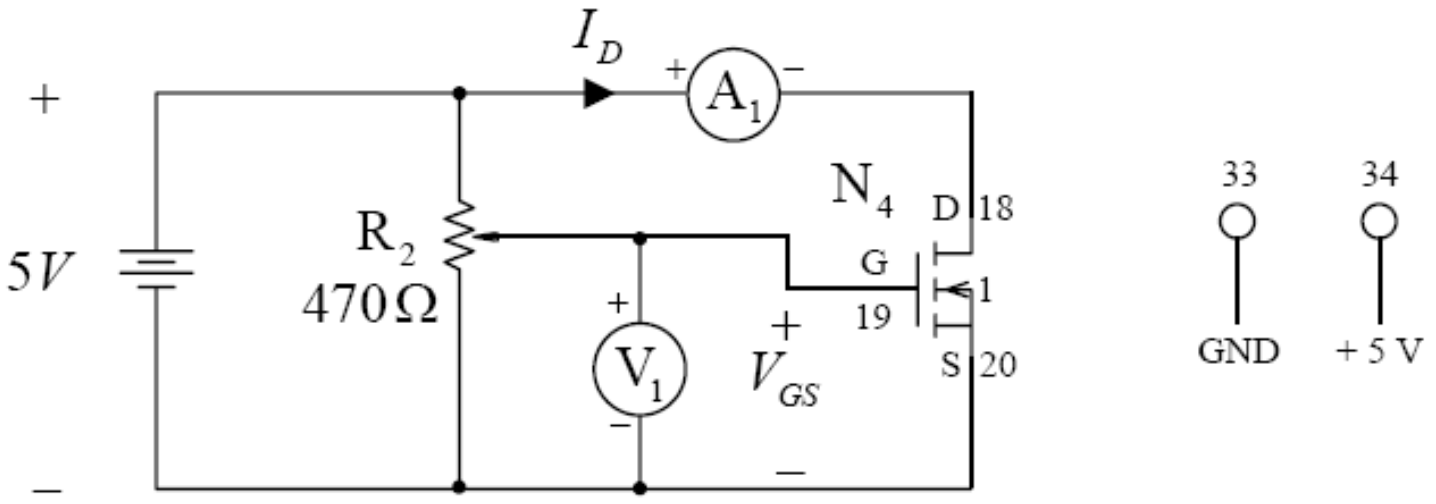


Figura 9 - Circuito a ser montado.

V_{GS}	V_{GS} medido	I_D	V_D	R_{DS}
0,0				
0,5				
1,0				
1,5				
2,0				
2,5				
3,0				
3,5				
4,0				
4,5				
5,0				

Parte experimental – Portas lógicas

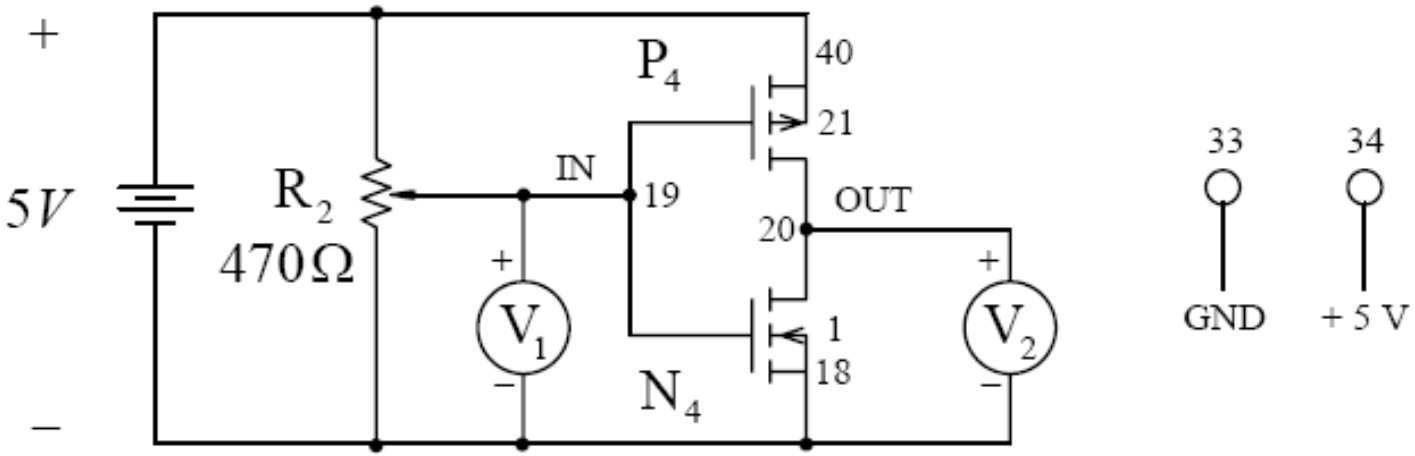


Figura 10 - Circuito a ser montado.

Vi	$V_i = V_1$ medido	$V_o = V_2$
0,0		
0,5		
1,0		
1,5		
2,0		
2,5		
3,0		
3,5		
4,0		
4,5		
5,0		